Extended Abstracts of the 20th (1988 International) Conference on Solid State Devices and Materials, Tokyo, 1988, pp. 145-148

A-9-6

Characterization of Silicon Bipolar Devices Fabricated Using Very-Low-Temperature Plasma Process

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Studies have been carried out on microcrystalline silicon layers deposited on monocrystalline bases and the heterojunction devices fabricated using them. The μc-Si layers varied from a microcrystalline to epitaxial structure, depending on the substrate surface treatment and plasma-CVD conditions. The interface properties were primarily determined by recombination through interface defects. It was found that very thin interfacial oxides are effective in growing homogeneous, reproducible microcrystalline emitters and in fabricating bipolar transistors with a high current gain of 450.

§ 1. Introduction

Future silicon bipolar devices with very high speed will require a highly doped, thin base structure with a wide band-gap emitter[1]. Therefore, some exploratory studies have been conducted to fabricate silicon heterojunction bipolar transistors (HBT). Various wide band-gap materials have been utilized, including SIPOS[2], a-Si[3], a-SiC[4] and μc-Si[5-7]. Results have indicated the feasibility of Si HBT's with a current gain higher than that of current polysilicon emitter transistors. Among these materials, the microcrystalline(μc-Si) is the most suitable due to its high current gain and low resistivity. However, very little research has been reported on the μc-Si material itself, or on the interface properties between the material and the base.

This paper describes the effects of the substrate surface and plasma-CVD conditions on the structure and properties of μc-Si layers. The hetero-interfaces between the wide band-gap emitters and single crystal bases were investigated in detail by fabricating bipolar devices and measuring their performance.

§ 2. Experimental

Si emitter layers, including epitaxial ones, were grown on a (100), p-type base at low temperatures of 160 to 250°C using an ordinary plasma-CVD process[7]. The deposition gases were SiH_4, PH_3 and H_2. The SiH_4/H_2 and PH_3/SiH_4 molar ratios were 0.02 and 0.05, respectively. The total gas pressure was kept at 0.3 to 0.6 Torr. As for the Rf power density, it ranged from 0.2 to 0.8 W/cm^2.

The structural and electrical properties were obtained using TEM, RHEED, SIMS and sheet resistance measurements. The diodes and transistors were fabricated using ordinary device processing, except for the n-type emitters.

§ 3. Results and Discussions

3.1 Material analysis

The structural and electrical properties of microcrystalline Si have been reported to depend on both the substrate surface and plasma-CVD conditions, including the reactant gas compositions, RF power and substrate temperature[7,8]. Typical examples of the substrate surface effects are presented in Fig.1. Resistivity varied greatly

with the substrate surface conditions. The μc-Si layer on the fused quartz glass had the highest resistivity, while the layer on the single substrate just after a HF dip etch had the lowest value. In addition, the resistivity tended to increase slightly with annealing up to about 600°C. Then, it decreased significantly due to the structural changes in the layers.

The structural features of the as-deposited Si layers were investigated using TEM. Transmission electron diffraction of the 60-nm-thick layers on the single substrate surface provided a spot pattern of a single-crystal structure, as shown in Fig. 2. However, the TEM micrograph of the layer shows the existence of a linear or ring-like defect. It can also be considered that the single-crystal structure suddenly changed into a μc-Si or polycrystalline structure with an increase in layer thickness[7,8].

The structure of the Si layers on the oxidized Si surface was quite different, as shown in Fig. 3. The electron diffraction pattern consisted of vaguely defined rings and some random spots, evidence of a microcrystalline structure.

Impurity profiles of phosphorus and unintentionally doped species are presented in Fig. 4 for the epitaxial layer. The phosphorus and hydrogen concentrations ranged from 1 to 5×10^{21} cm^{-3}, but the hydrogen concentration decreased near the substrate surface. This kind of decrease, but to a lesser degree, also existed for the oxygen and carbon atoms. These results support the finding in the authors' previous paper that thinner layers have better crystallinity[7].

The active phosphorus concentration measured by the Hall method was 3×10^{20} cm^{-3}. This was about one-tenth of the total phosphorus concentration in the layers. In addition, fluorine atoms were found to increase at the interface between the Si layer and the substrate. This profile suggests that the fluorine bonded to the substrate surface during the HF dip treatment before deposition.

3.2 Device analysis

Interface properties are expected to affect junction characteristics, especially under low forward current and reverse bias conditions. Representative J-V characteristics for diodes with μc-Si and epitaxial emitters are given in Fig. 5. From this figure, it is impossible to determine the existence of wide band-gap heterojunction effects. Nevertheless, the effects of the plasma-CVD conditions on diode characteristics can be ascertained. The diodes with the epitaxial emitters tended to have a relatively high generation-recombination current as compared to that of the μc-Si emitters.

The reverse characteristics for the diodes with the epitaxial emitter are presented in Fig. 6, which uses a log-log plot. Saturated or linear reverse characteristics appeared under low reverse bias conditions followed by a power law dependence of the current on voltage. The reverse current is probably related to the tunneling of carriers at interface defects in the space-charge region. The difference between the μc-Si and epitaxial emitters is presumably due to lower defect densities because of higher bonded hydrogen concentrations at lower growth temperatures.

To clarify the recombination mechanism around the junctions, diode saturation current density was examined as a function of measurement temperature. The saturation current density decreased linearly with the reciprocal temperature and the n value was almost constant, as shown in Fig. 7. The activation energy was 0.47 eV, about half that of the silicon band-gap. This suggests that recombination prevails in the space charge regions of the emitter structure.

The epitaxial and μc-Si n-type layers were utilized as emitters to fabricate npn bipolar transistors with an emitter area of $20\times20\,\mu m^2$.

The change in current gain of fabricated transistors with substrate surface treatment is presented in Table 1.

Table 1 Effects of substrate surface treatment on current gain of transistors fabricated using emitter layers deposited on p-type base at 250°C

Substrate surface treatment	Structure	h_{FE} Mean(Max)
RCA → HF	Epitaxy	45(60)
RCA	Microcrystalline	370(450)

Lower current gains were obtained for the transistors with the epitaxial emitter fabricated on the p-type base after RCA cleaning and a HF dip. The values were almost the same as those of diffused npn transistors. This shows that the emitter has a similar epitaxial structure.

A high-performance μc-Si emitter structure was fabricated on a p-type surface cleaned and chemically oxidized in the RCA solution using the epitaxial growth condition. Figure 8 shows that the maximum current gain was 450 at a collector current of 1×10^{-2} A for the transistor, which had a base sheet resistance of 12kΩ. This gain is superior to that of conventional polysilicon emitter transistors. The gain is probably due to the existence of the thin interfacial oxide layer and a microcrystalline wide band-gap layer on it.

Acknowledgments

The authors are grateful to Dr. Toshikazu Shimada for his discussion on μc-Si and to Drs. Masanobu Miyao and Thoru Nakamura for aid in fabricating and analyzing the bipolar transistors.

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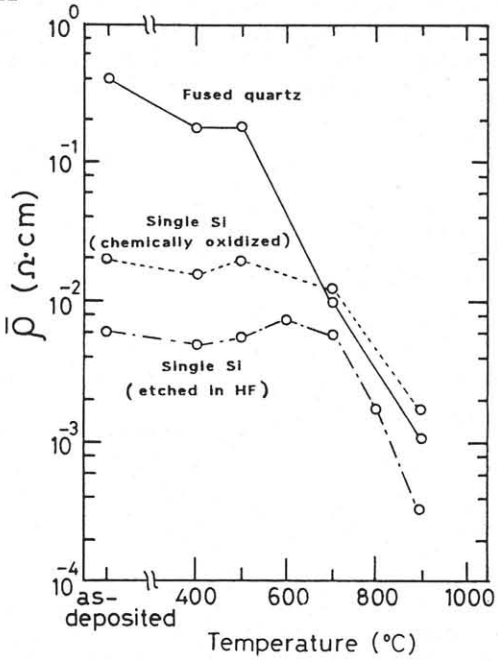

Fig.1 Effects of substrate surface conditions and annealing on resistivities of plasma-CVD layers.

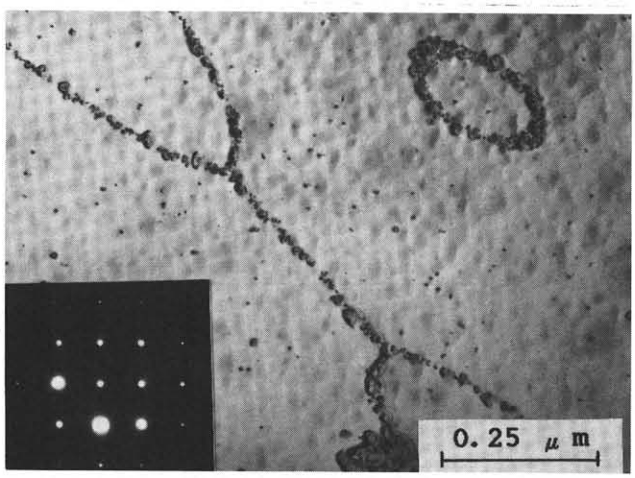

Fig.2 TEM micrograph and electron diffraction pattern of 60-nm-thick epitaxial layer grown at 255°C on substrate surface just after a HF dip etch.

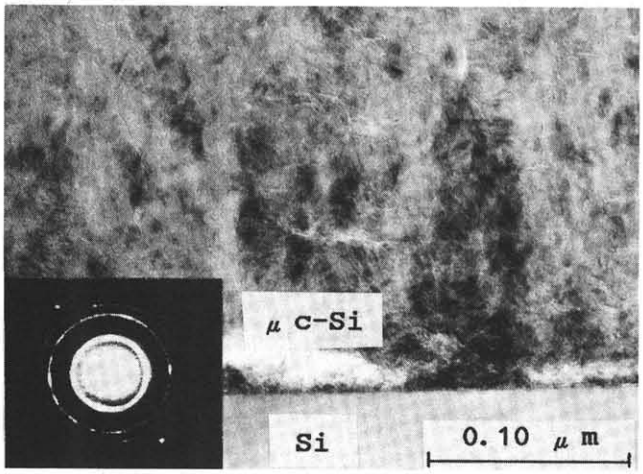

Fig.3 Cross-section transmission electron micrograph and diffraction pattern of a μc-Si layer grown on a chemically-oxidized surface deposited at 160°C.

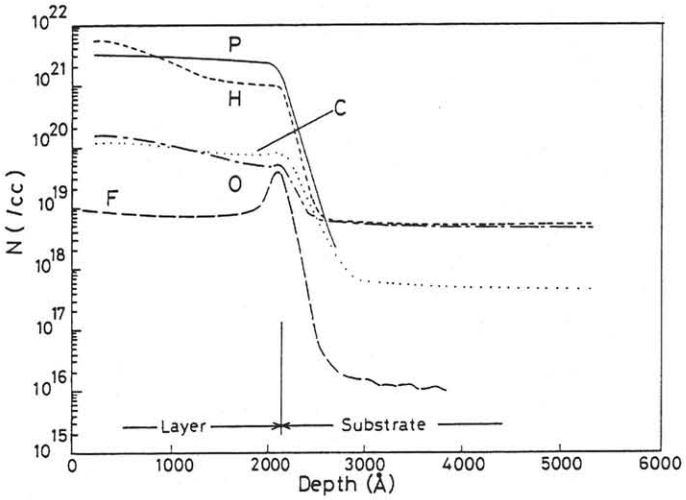

Fig.4 SIMS impurity profiles for phosphorus-doped layer grown at 230°C.

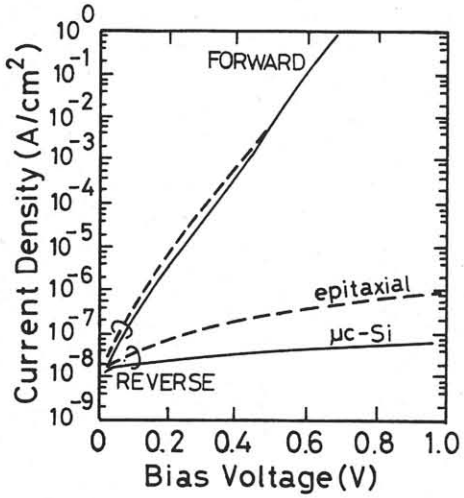

Fig.5 J-V characteristics of diodes with microcrystalline and epitaxial layers.

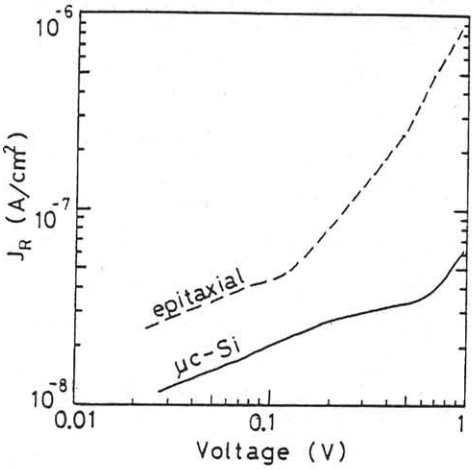

Fig.6 lnJ vs. lnV under reverse bias conditions for diodes with epitaxial and μc-Si emitters.

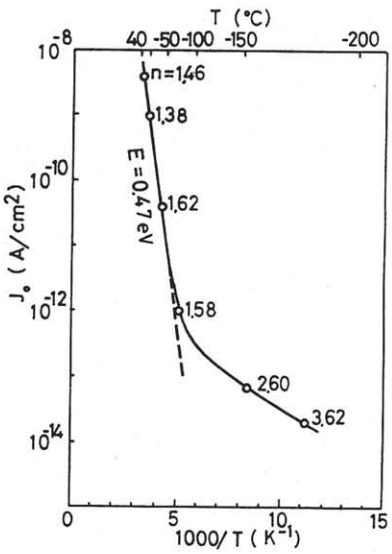

Fig.7 Change in diode saturation current density with reciprocal measurement temperature.

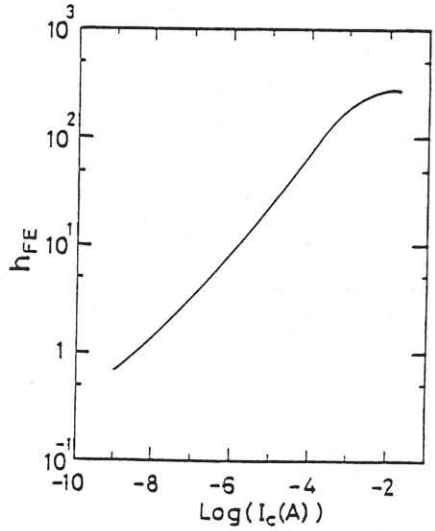

Fig.8 Relationship between current gain and collector current.
(emitter area: 400 μm²)