

The Integration of Double-Polysilicon NPN Transistors in an Analog BiCMOS Process

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The integration of high performance npn transistors with the self-aligned double-polysilicon structure provides a concept for second generation BiCMOS processes. The integration can be achieved by adding three mask levels to a first generation BiCMOS process. The integrity of the emitter-base spacer is shown to be improved by applying a combined isotropic and anisotropic etching process to etch the first polysilicon layer. To optimize the process for analog applications, the epilayer thickness and n-well doping were varied, and a comparison was made between polysilicon emitters and epitaxial emitters grown by molecular beam epitaxy.

1. BiCMOS PROCESS INTEGRATION

The packing density and the power dissipation of a mixed analog-digital BiCMOS circuit are mainly determined by the CMOS part of a BiCMOS process, whereas the speed and driving capability are mainly determined by the performance of the bipolar transistors. The integration of self-aligned bipolar transistors into a BiCMOS process provides a way to upgrade the performance of a BiCMOS technology to a level comparable to that of advanced pure bipolar technologies.

The use of sidewall spacers along poly-Si is an effective way to combine LDD-MOS devices with self-aligned bipolar npn transistors with the double-poly structure. In fact three masking levels have to be added to a first generation BiCMOS process to integrate the double poly npn transistor:

- 1) buried contacts to p+ poly-Si for the base contacts of the npn transistor
- 2) p+ poly-Si (base contacts) vs. n+ poly-Si (MOS gates) definition
- 3) the second poly-Si (emitter) definition.

Figures 1a and 1b show SEM cross-sectional

views of the resulting bipolar and MOS devices. Since the CMOS parameters are not different from those of a standard CMOS process, they will not be discussed here. Some of the bipolar parameters will be dealt with in this paper.

2. SIDEWALL SPACER TECHNOLOGY

The width of the oxide sidewall spacer in a BiCMOS process is a critical parameter since it not only determines the efficiency of the LDD structure, but it also determines the emitter-base sidewall junction, which is the most critical part of a self-aligned npn transistor.

The integrity of the emitter-base spacer is critically influenced by the processing steps that define the buried contacts for the second poly. Both the overetch that is necessary to open the emitter areas, and the HF-dip prior to the second polysilicon deposition tend to thin the emitter-base spacer to a minimum thickness of well below 0.1 μm at the upper corner, as shown in figure 2a. This leads to a serious reduction of the

process capability and potentially to yield loss. The spacer width itself cannot be corrected for this effect, since it is fixed by the LDD requirements. A thicker interpoly oxide would give a slight improvement in the spacer structure, as shown in figure 2b, but at the cost of deeper contacts to the first polysilicon.

Figure 3a shows the result obtained by applying a two step etching process to etch the first polysilicon layer: the first part of the polysilicon is etched isotropically in a mixture of CF₄ and O₂ (see fig.3b), and the rest of the polysilicon is etched anisotropically in a Cl₂ plasma. This produces a partial undercutting of the polysilicon which is filled with oxide during the deposition of the spacer layer. As shown in figure 3a this gives a considerable improvement of the spacer integrity at the critical point. From the device evaluation it appears that the interpoly isolation is improved and that the occasional occurrence of non-ideal emitter-base junctions is reduced as well.

d-epi (μm)		2.25	2.50	2.75
hfe	NW1	140	140	140
	NW2	120	120	120
Vearly (V)	NW1	25	25	25
	NW2	35	50	50
ft (GHz)	NW1	5.0	4.4	--
	NW2	4.5	4.0	--

Table I. AC and DC npn parameters for various epilayer thicknesses and n-well doping levels. (NW1: CMOS n-well conc. NW2: 1/3 * NW1 conc.)

3. NPN COLLECTOR OPTIMIZATION

In analog applications not only the AC performance is important, but also the DC performance. The basic electronic requirements are a maximum cut-off frequency (ft) at a given product of current gain (hfe) and Ear-

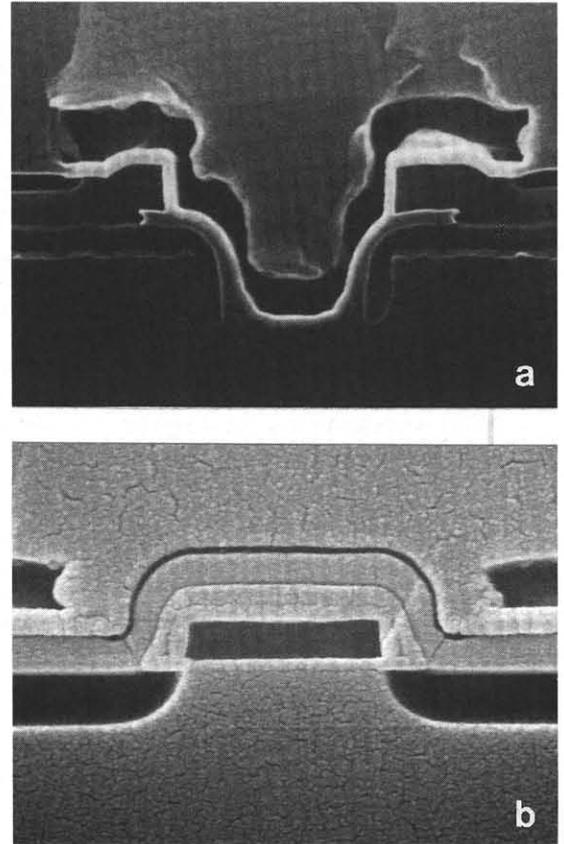


Fig.1. SEM views of self-aligned npn transistor (a) and LDD MOS transistor (b).

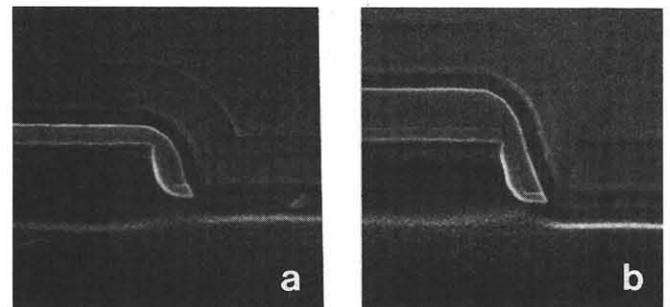


Fig.2. SEM views of emitter-base spacer: a) conventional b) thick interpoly oxide

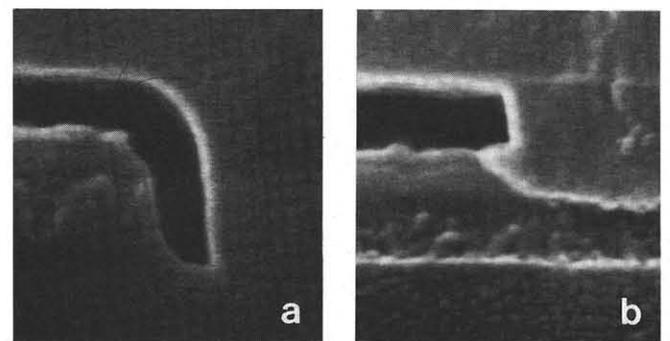


Fig.3. SEM views of emitter-base spacer: a) spacer using two step process b) after isotropic poly etch

ly voltage (Vearly) of at least 4000 V. Table I shows the experimental results of the collector optimization: an initial epilayer thickness of 2.5 μm and an n-well doping level of about $1\text{E}16\text{ cm}^{-3}$ (i.e. a factor 3 below the CMOS n-well) seem to be appropriate. The corresponding effective collector thickness is about 1.5 μm .

4. SIMULATION OF EPITAXIAL EMITTERS

It is well known that polysilicon emitters can be applied to obtain shallow emitters in high frequency transistors. It is also known that the presence of some oxygen at the poly-mono interface tends to increase the emitter Gummel number at the cost of a serious increase in emitter series resistance. If this effect is avoided, the Gummel number of a polysilicon emitter is generally low and limits the DC device performance. The straightforward alternative solution of increasing the emitter-base junction depth is unattractive since the emitter-base sidewall junction increases accordingly. An epitaxial emitter grown between the oxide spacers, could be used to increase the emitter efficiency without increased sidewall effects. To simulate the relative effects of polysilicon emitters and epitaxial emitters one-dimensional process and device simulations were used. In all cases it was assumed that the emitter-base junction depth extends 50 nm below the oxide spacer i.e. that the parasitic sidewall effects are equally small in both cases. Therefore one-dimensional simulations will give a good prediction of the actual relative transistor performances. A hypothetical device structure was defined consisting of the following layers that were all assumed to be grown by epitaxy at 800°C:

- 1) A buried layer with a doping level of $2\text{E}19\text{ cm}^{-3}$.
- 2) A collector layer with a variable dope (Nd) and thickness (x):

Nd(cm-3)	x(μm)
3E16	0.25, 0.50, 0.75, 1.00
1E16	0.25, 0.50, 0.75, 1.00, 1.25
5E15	1.25, 1.75

- 3) A 50 nm thick base layer with a uniform doping level of $2\text{E}18\text{ cm}^{-3}$
- 4) A 50 or 200 nm thick emitter with a uniform doping level of $2\text{E}20\text{ cm}^{-3}$
- 5) A metal contact on top of the emitter with a recombination velocity of $3\text{E}5\text{ cm/s}$ i.e. no reduction of hole recombination due to interfacial oxides.

The 50 nm emitter represents a polysilicon emitter and the 200 nm emitter an epitaxial emitter.

Figure 4 shows the resulting correlation between f_t and $h_{fe} \cdot V_{early}$ for both emitter structures. As expected the MBE-Si emitter has a better DC performance due to the increased emitter efficiency, but a slightly decreased AC performance because of the increased hole storage in the emitter.

From the simulations it can be concluded that a demand for a minimal product of current gain and Early voltage of 4000 V limits the cut-off frequency to about 10 GHz, even for an idealized transistor structure, and that an epitaxial emitter provides a way to realize such a transistor.

5. NPN EMITTER EXPERIMENTS

As a first experiment for the optimization of the emitter, polysilicon emitters with and without interfacial oxides were compared with epitaxial emitters grown by molecular beam epitaxy (MBE). The TEM micrograph in figure 5 clearly shows that the MBE-Si layer is epitaxial in the emitter area and polycrystalline outside the emitter area. Figure 6 shows the results of the emitter series resistance measurements on $4\text{ }\mu\text{m}^2$ emitters. The MBE-Si emitter has the lowest series resistance, the value for the polysilicon emitter without interfacial oxide is

marginally higher and the resistance for the polysilicon emitter with the interfacial oxide is significantly higher.

It was found that the base saturation currents vary accordingly: the MBE-Si emitter has a slightly higher base current than the polysilicon emitter without interfacial oxide and the polysilicon emitter with interfacial oxide has a base current which is about a factor 4 lower. Obviously the high series resistance in this emitter makes its practical application doubtful.

The epitaxial emitter can be used to provide a high emitter efficiency (by increasing the layer thickness) without increasing the emitter-base sidewall capacitance, since most of the emitter is contained between the oxide sidewall spacers.

5. CONCLUSION

The combination of self-aligned npn transistors with LDD MOS technology provides a high performance BICMOS process for mixed analog/digital applications. The integrity of the sidewall oxide spacers can be improved by applying a two step process to etch the first polysilicon layer.

The thickness of the epilayer and the doping concentration of the n-well were optimized to meet the DC requirements of the npn transistors. The use of an epitaxial emitter rather than a polysilicon emitter allows an increased cut-off frequency at a given product of current gain and Early voltage.

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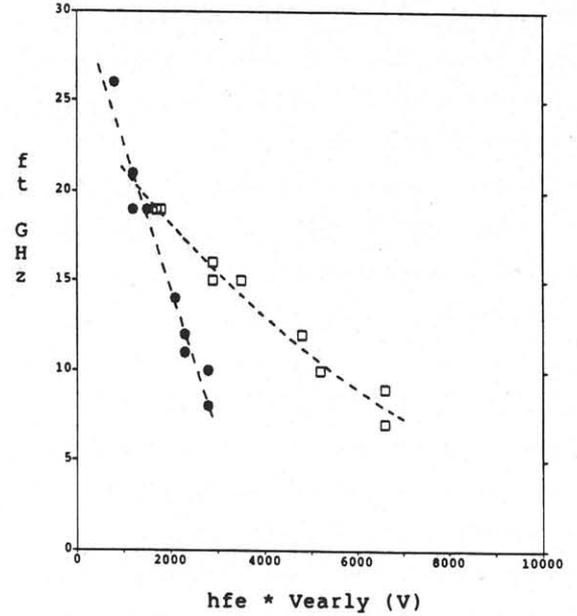


Fig.4. Simulated relation between f_t and $h_{fe} \cdot V_{early}$ for poly-Si and epitaxial emitters (● poly-Si, □ MBE-Si).

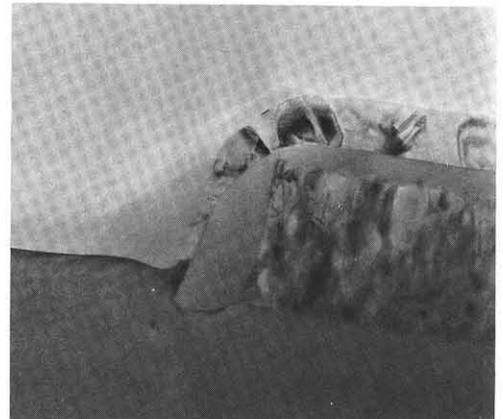


Fig.5. TEM cross-section of MBE emitter.

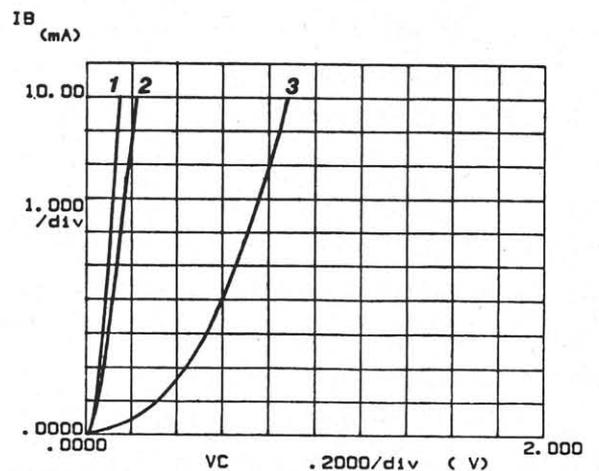


Fig.6. Emitter series resistance measurements (emitter area $4 \mu\text{m}^2$):
 1: MBE-Si 2: poly-Si
 3: poly-Si with interfacial oxide.