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An Experimental Study of Hot Carrier Temperature in Submicron pMOSFETs

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This paper shows hot carrier effects in pMOSFETs. The gate current, in pMOSFETs, consists of electrons generated by impact ionization in bulk, the same as in nMOSFET. The electron temperature, in pMOSFETs, is first determined experimentally. It is $2430K$ at $V_d = -5V$, and $2650K$ at $V_d = -6V$. The temperature is almost independent of the gate oxide thickness and the gate length. Through the experiments, it can be deduced that electrons strongly interact with holes.

1. Introduction

Most of the work on the hot carrier in MOSFET has been reported for n-channel devices. In the work, electrons, which are majority carriers, are mainly investigated, and holes, which are minority carriers, are not taken into consideration. In CMOS structure, however, p-channel MOSFET is merged, so attention should also be paid to the p-channel device. Moreover, with the reduction in device dimensions, not only majority carriers but also minority carriers will play important roles in device operation.

The purpose of this work is to show an experimental analysis of the hot carrier phenomenon in pMOSFET with a surface channel structure. Analyzing gate and substrate currents of pMOSFETs which are experimentally obtained, electron temperature in the pMOSFETs can be determined for the first time. Through the experiments, it can be deduced that both carriers strongly interact.

2. Sample Preparation

The samples of pMOSFET are fabricated using Boron doped poly-sillicon gate technology with oxide thicknesses of 5 to $10nm$. The gate length is varied from 0.4 to $1.2\mu m$. After a SiO_2 side wall of $100nm$ is formed, an $0.24\mu m$ p^+ junction is made. Channel doping conditions are the same for all measured samples; the n-type substrate impurity concentration is $7 \times 10^{16} cm^{-3}$, and the phosphorus channel doping condition is $3.0 \times 10^{12} cm^{-2}$ at $25keV$. Using the two-dimensional simulator, *TRANAL*,[1] all pMOSFETs used here are confirmed as operating in the surface channel mode.

3. Results and Discussions

In Fig. 1, the maximum substrate electron current ($I_{sub,max}$) is shown as a function of $1/(V_d - V_{dsat})$ for various devices. Here, V_d is a drain voltage and V_{dsat} is a potential at the pinchoff point. The figure shows for the pMOSFETs with $5nm$ gate oxide for the different gate length; 0.38, 0.76, and $1.19\mu m$. It also includes the results for pMOSFETs with $0.76\mu m$ gate length for the different gate oxide thickness; 5, 7 and $10nm$. From the figure, it can be seen that all data points fall mostly on a single straight line. This result shows that the impact ionization takes place independently of the gate oxide thickness and the channel length in pMOSFETs as in nMOSFETs. Therefore, I_{sub}

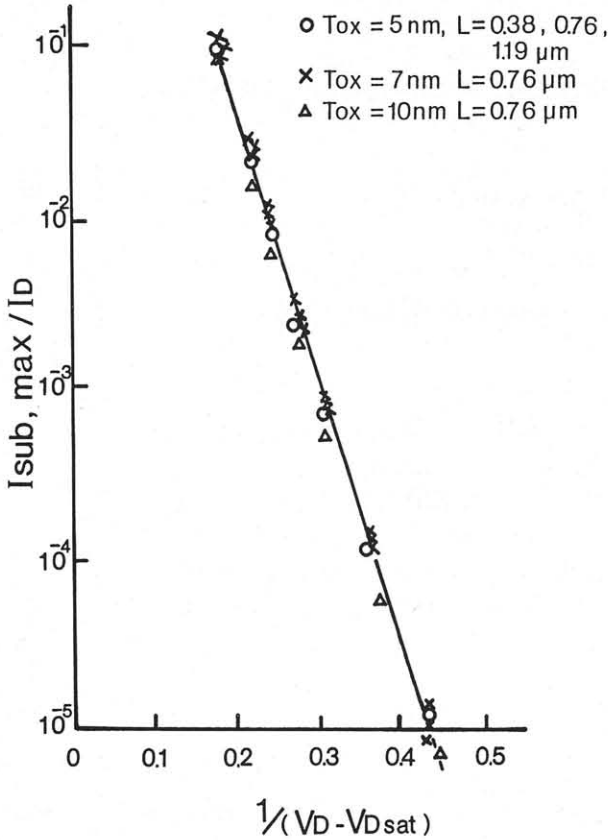

Fig.1 Substrate current characteristics for pMOSFET with surface channel structure.

is formulated by an expression similar to that for nMOSFETs reported by C. Hu et al.[2].

$$I_{sub} = M(T_h)I_d exp(-\phi_i/kT_h) \quad (1)$$

where T_h is a hole temperature proportional to $V_d - V_{dsat}$. M is a variable related to the average hole (majority carrier) temperature, although Hu assumed it to be constant ($M = 2$).

The gate current in pMOSFETs is confirmed as electron conduction and the maximum current is given for the condition $|V_g| < |V_d|$. As the substrate current is due to electron conduction, the gate current is caused by the injection of electrons generated by impact ionization.

The carriers' distribution in the high field region can be assumed to be drifted Maxwellian.[3] If the energy distribution of the minority carriers in the surface channel is also assumed to be drifted Maxwellian, the gate current can be written with eq. (2).

$$I_g = I_{sub} exp[-(\phi_b - \xi - \zeta)/kT_e]$$
$$= I_{sub} exp(-\phi_b/kT_e) exp[(K'/kT_e)/\sqrt{T_{ox}}] \quad (2)$$

where T_e is the averaged electron temperature. In the equation, an important result from Fig. 1 that the minority carrier temperature is independent of the gate oxide thickness and the channel length, but is dependant only on the drain voltage, is used. The barrier height lowering effect of $Si - SiO_2$ interface is taken into account. A band diagram of $Si - SiO_2$ system is depicted schematically in Fig. 2. Here, ξ is a factor due to image force lowering and ζ is a factor for Fowler-Nordheim tunneling through SiO_2. ξ is in proportional to $1/\sqrt{T_{ox}}$. Although ζ cannot be expressed by a simple equation, the effect of Fowler-Nordheim tunneling is implicitly taken into account through K', which can be determined by experiments. In Fig. 3, ex-

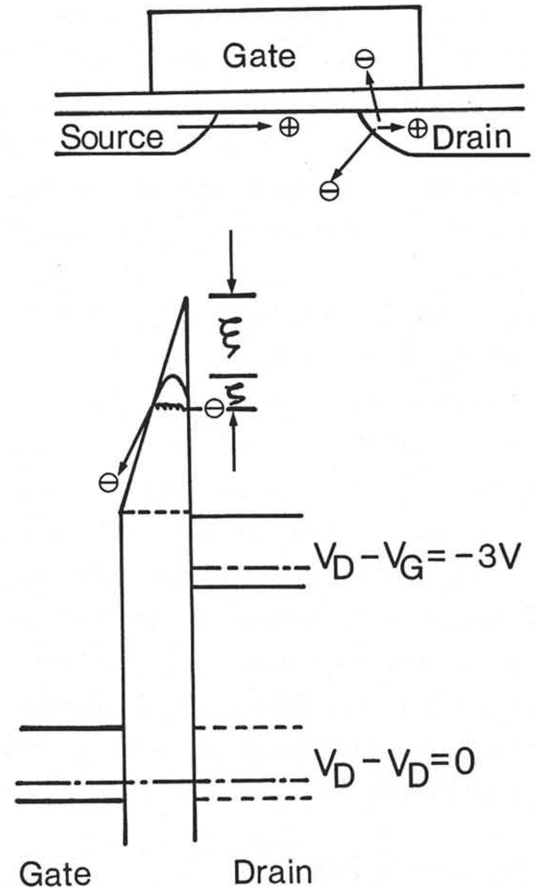

Fig.2 Considered model for gate current. ξ is a factor of image force lowering, and ζ ia a factor of Fowler-Nordheim tunneling.

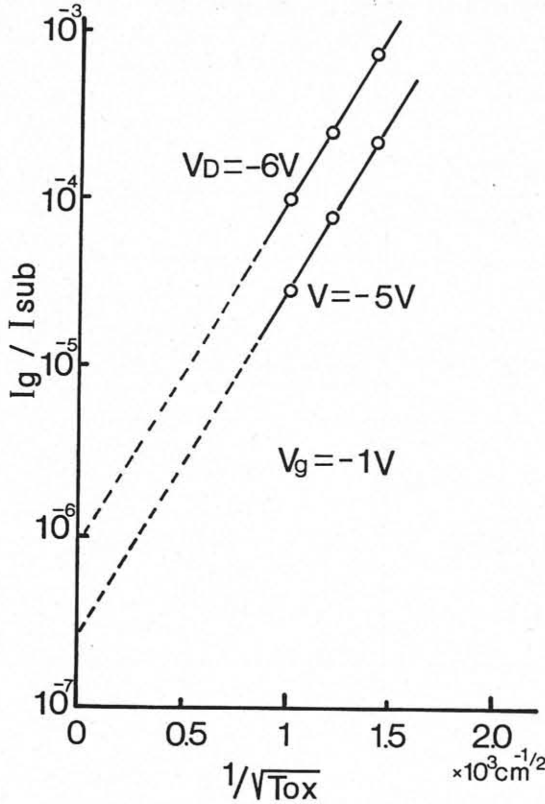

Fig.3 Gate current dependency on gate oxide thickness. An intersection of y-axis gives $exp(-\phi_b/kT_e)$, and a slope gives K'/kT_e.

perimental relationships of I_g/I_{sub} *vs.* $1/\sqrt{T_{ox}}$ are given for two drain applied voltages, $V_d = -5V$ and $V_d = -6V$. These results are expressed by the straight line, as was expected in eq. (2). The values of ϕ_b and K'/kT_e are determined from these experimental results. Using the barrier height of 3.2eV, measured by Fowler-Nordheim injection,[4] $kT_e = 0.21eV$ at $V_d = -5V$ and $kT_e = 0.23eV$ at $V_d = -6V$ are obtained. They correspond to electron temperatures of $2430K$ and $2650K$, respectively. These temperatures are mostly consistent with the measurement for nMOSFETs by Toriumi et al.[5]

From equations (1) and (2),

$$I_g/I_d \propto (I_{sub}/I_d)^n \quad (3)$$

where

$$n = [(\phi_b - \Delta\phi)/kT_e + \phi_i/kT_h]/(\phi_i/kT_h) \quad (4)$$

and

$$\Delta\phi = \xi + \zeta \quad (5)$$

A typical result on I_g/I_d *vs.* I_{sub}/I_d for $T_{ox} = 5nm$ is shown in Fig. 4. A value of n is 2.45 ± 0.05 for the different oxide thickness. If the temperatures of the holes and electrons are determined from their phonon mean free pathes, which are $5.5nm$ for holes and $7.6nm$ for electrons,[6] a calculated ϕ_i cannot be accepted because it is less than the forbidden gap energy. When assuming $T_e = T_h$, the calculated parameters are summarized in Table I. In this case, the values for ϕ_i are well consistent with the silicon forbidden gap energy. The result suggests that the electrons and the holes interact strongly so that their average temperature becomes nearly equal.

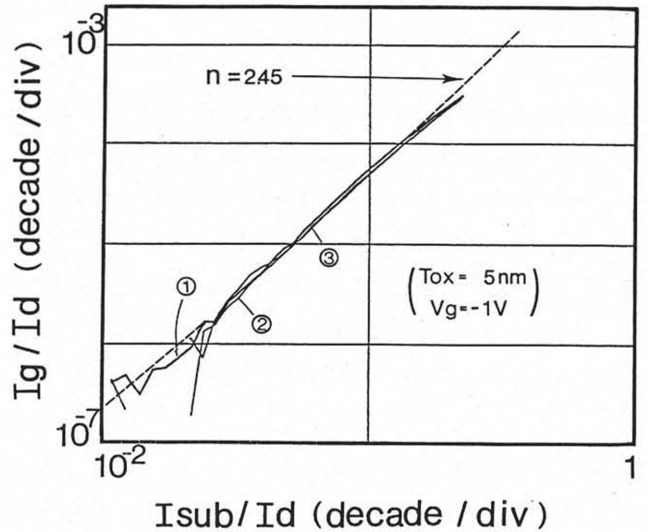

Fig.4 Measured example of I_g/I_d *vs.* I_{sub}/I_d relationship for pMOSFET with $5nm$ gate oxide.

4. Summary

1. Impact ionization takes place independently of the gate oxide thickness and the channel length in pMOSFET as well as in nMOSFET.
2. The gate current in pMOSFET is confirmed as mainly due to electrons generated by impact ionization.

Table I Measured parameters and estimated results of $M, kT_e, \Delta\phi$, and ϕ_i on the assumption that $\phi_b = 3.2eV$ and $T_e = T_h$.

Measured Parameters	$[(\phi_b - \Delta\phi)/kT_e$ $+\phi_i/kT_h]/(\phi_i/kT_h)$	2.45 ± 0.05	
		$V_d = -5V$	$-6V$
	ϕ_b/kT_e K'/kT_e ϕ_i/kT_h	15.2 4.72×10^{-3} $-ln(2.1 \times 10^{-2}/M)$	13.9 4.65×10^{-3} $-ln(8.6 \times 10^{-2}/M)$
Estimated Values	M kT_e $\Delta\phi(at\ T_{ox} = 5nm)$ ϕ_i	7.6 $0.21eV$ $(T_e = 2430K)$ $1.41eV$ $1.23eV$	13.6 $0.23eV$ $(T_e = 2650K)$ $1.51eV$ $1.16eV$

3. The electron temperatures (the minority carrier temperatures) for pMOSFET are experimentally determined to be $2430K$ at $V_d = -5V$ and $2650K$ at $V_d = -6V$.
4. The results suggest that the majority and minority carriers interact strongly so that their temperatures become nearly equal.

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