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Experimental Evidence for Hole-Induced Interface State Generation under High Field Tunneling Current Stressing

Yoshio OZAWA, Masao IWASE, and Akira TORIUMI

ULSI Research Center, Toshiba Corporation,
1 Komukai-Toshiba-cho, Saiwai-ku, Kawasaki 210, Japan

Interface state generation, due to tunneling current injection from the inversion layer into the gate oxide, was investigated. It was found that the generated interface state density is linearly related with the substrate hole current, regardless of the oxide field or the oxide thickness. The results obtained in this work provide strong evidence that interface state generation is triggered by holes passing through the $Si-SiO_2$ interface, even in electron injection. The interface state generation is also discussed as a function of applied voltage in electron injection.

1. INTRODUCTION

Electron injection into the gate oxide in MOS structures generates interface states at the $Si-SiO_2$ interface, which cause threshold voltage shift and transconductance degradation. Several models have been proposed to explain the interface state generation mechanism. Among them, a model in which holes have a strong influence on the interface state generation at $Si-SiO_2$ has been proposed[1,2]. Direct evidence for this model, however, has not yet been reported.

This paper presents experimental evidence for hole-induced interface state generation under Fowler-Nordheim (F-N) tunneling current stressing.

2. EXPERIMENTAL RESULTS

The samples used in this study were conventional n^+ poly-silicon gate n-channel MOSFETs, fabricated on 3 ohm cm (100) p-type Si wafers. The gate oxides were grown in a dry O_2 ambient at 900 °C to thicknesses from 5.5 to 55 nm. Small devices, whose channel length was 4 um, were used, since large area oxides may have some extrinsic defects.

Figure 1 illustrates schematically the experimental arrangement for oxide stressing. The gate electrode was positively biased and F-N tunneling current was injected from the inversion layer. The current injection was implemented under low electron fluence conditions to clarify the elementary process for interface state generation. The interface state density was evaluated by the charge pumping technique[3]. The experimental setup for the measurement is shown in Fig.2. Gate pulses, with a frequency of 100 kHz, were used in this experiment and sensitivity of $1x10^9$ cm^{-2} eV^{-1} was obtained for measuring the interface state density, which was limited by the junction leakage current.

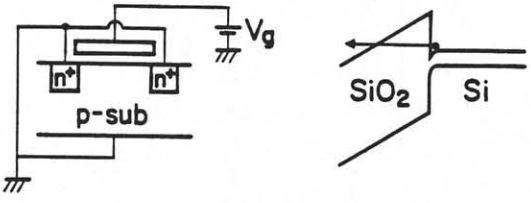

Fig.1 Experimental arrangement and schematic band-structure diagram for F-N current injection.

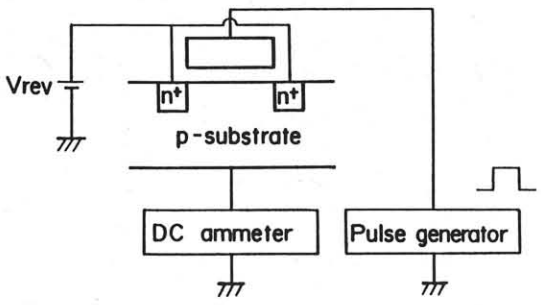

Fig.2 Experimental setup for charge pumping measurements.

Degradation under low electron fluence conditions was investigated as a parameter of oxide thickness. As shown in Fig. 3, the generated interface state density, $\Delta\overline{Dit}$, was linearly related to the electron fluence, Ninj, except for a 5.5 nm oxide. A moderate dependence on Ninj for the 5.5 nm oxide is discussed in the next section. Figure 4 shows the oxide thickness dependence of $\Delta\overline{Dit}$ under two different oxide fields. Above 20 nm thickness, $\Delta\overline{Dit}$ decreases linearly with the oxide thickness decrease. On the other hand, $\Delta\overline{Dit}$ deviates from this linearity when the oxide thickness becomes thinner than 20 nm. Such characteristic behavior was also seen in the oxide thickness dependence of the substrate hole current observed in F-N tunneling current injection[4].

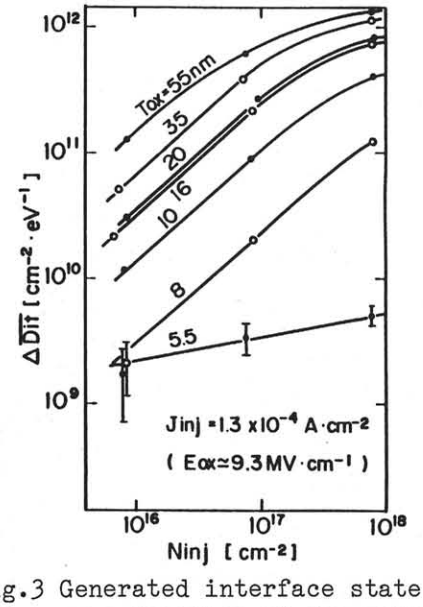

Fig.3 Generated interface state density as a function of the number of injected electrons for various gate oxide thicknesses.

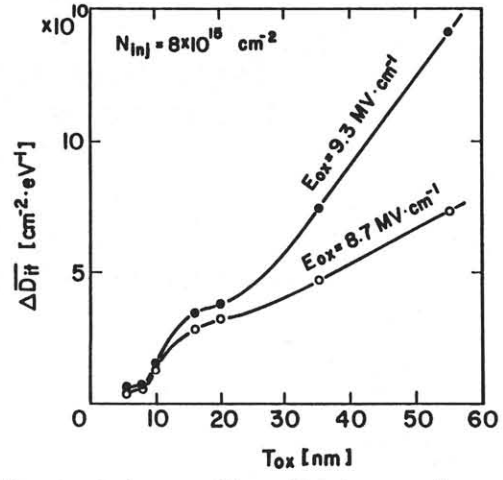

Fig.4 Gate oxide thickness dependence of the interface state density generated by F-N tunneling current injection at two fixed oxide fields.

This fact suggests that the existence of holes is essential for the interface state generation, though electrons are injected into the Si-SiO_2 interface.

In order to clarify the relationship between $\Delta\overline{Dit}$ and the number of holes, the number of generated interface states per unit area, ΔNit, was investigated as a function of the number of holes passing through the Si-SiO_2 interface, Nhole. The results are shown in Fig.5 for various oxide thicknesses under three different oxide fields.

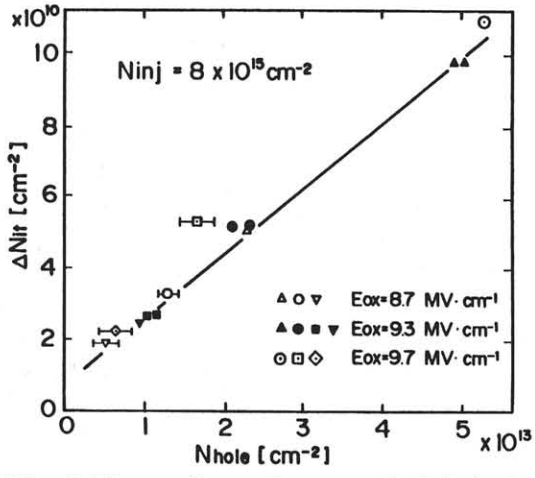

Fig.5 The number of generated interface states per unit area as a function of the number of holes passing through the Si-SiO_2 interface for gate oxides of 10 nm(◇), 16 nm(▽,▼), 20 nm(□,⊡), 35 nm(○,●,⊙) and 55 nm(△,▲) under three different oxide fields.

Nhole was evaluated from the substrate hole current observed in F-N tunneling injection. It is noted that the generated interface state density is linearly dependent on Nhole, regardless of the oxide field or the oxide thickness. This result provides a strong evidence that interface state generation is caused by holes passing through the Si-SiO_2 interface. The interface state generation efficiency by a hole was found to be about 2×10^{-3}, from the slope indicated in Fig.5.

3. DISCUSSION

The hole generation mechanism under high field electron injection is first discussed. In thick oxides, the mechanism via interband impact ionization has been usually mentioned, because an applied voltage is high enough to cause impact ionization in SiO_2. On the other hand, in thin oxides, which are typically 10 nm or less, injecting electrons cannot gain energy to bring about the hole generation in SiO_2 by the impact ionization process. Therefore, another mechanism is to be considered. Fischetti proposed a model in which holes are generated via interface plasmon emission at the interface between the oxide and the gate electrode[5]. It is noticed in this model that there should be some threshold energy to excite interface plasmon. From this point of view, the minimum voltage applied across the oxide for interface state generation was investigated under low electron fluences. Figure 6 shows $\overline{\Delta Dit}$ as a function of the voltage applied across the oxide, Vox. It is clearly shown that there is a threshold of about 6.8 V in Vox to generate the observable interface states[6]. On the other hand, the interface plasmon energy at Si-SiO_2 has been reported to be about 7.7 eV by LEELS[7,8]. Taking into account the

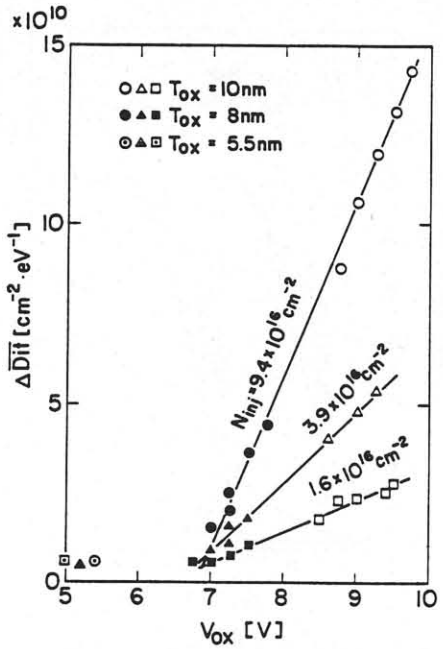

Fig.6 Generated interface state density as a function of applied voltage across the SiO_2 for gate oxides of 5.5 nm, 8 nm and 10 nm. Results are shown for three kinds of electron fluences.

plasmon energy width, the threshold value of 6.8 V seems to support the interface plasmon model for interface state generation, though it is not definitely concluded.

Next, interface state generation under stressing voltage below 6.8 V is discussed. If the mechanism considered above is dominant for interface state generation in thin oxides, interface states should not be generated in F-N tunneling injection with Vox lower than 6.8 V. Experimental results, however, showed that the increase of the interface state density was observed under electron fluences higher than 10^{18} cm^{-2}, even though Vox was lower than 6.8 V. The results are shown in Fig. 7. It is also found that $\overline{\Delta Dit}$ is not proportional to Ninj under low applied voltage conditions, as shown in Fig. 8. Therefore, the interface state generation mechanism under low applied voltage conditions (Vox < 6.8 V) seems to be different from that under higher applied voltage conditions.

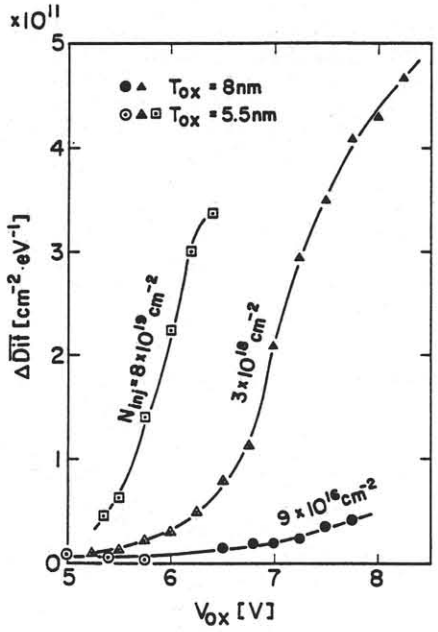

Fig.7 Generated interface state density as a function of applied voltage across SiO_2 for electron fluences up to 8×10^{19} cm^{-2}.

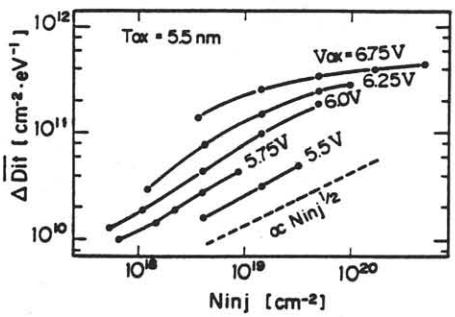

Fig.8 Generated interface state density as a function of the number of injected electrons for various applied voltage across SiO_2.

4.SUMMARY

This paper has reported on three observations concerning interface state generation due to Fowler-Nordheim tunneling current injection into the gate oxide.

(1) Gate oxide thickness dependence of $\Delta\overline{Dit}$ showed a characteristic behavior similar to that for the substrate hole current.

(2) $\Delta\overline{Dit}$ was linearly related to the substrate hole current, regardless of the oxide field or the oxide thickness. The interface state generation efficiency by a hole was found to be about 2×10^{-3}.

(3) The applied voltage across the gate oxide, to generate the observable interface states, had a threshold of 6.8 V, which supports the interface plasmon model for interface state generation.

These observations indicated that the interface state generation is triggered by holes passing through the $Si-SiO_2$ interface, even in electron injection. The authors have also discussed the interface state generation under low applied voltage conditions. From the viewpoint of the relationship between $\Delta\overline{Dit}$ and Ninj, it was suggested that there is another kind of interface state generation mechanism for Vox lower than 6.8 V.

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