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New Phenomena in MNOS Retention Characteristics and Their Application to Memory Device Design for Megabit EEPROM's

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An MNOS memory device design for Megabit EEPROM's has been developed. Shrunk MNOS devices are closely evaluated. While charge retentivity of the erased-state depends slightly on Si_3N_4 thickness, written-state retentivity is improved by reducing Si_3N_4 thickness. These new phenomena are applied to memory device design. It is shown that 1M bit MNOS EEPROM can be designed with Si_3N_4 thickness 20.0 nm and programming voltage 10.7 V. These results show the MNOS device to be a very promising candidate for Megabit EEPROM's.

1. Introduction

Currently, EE(Electrically Erasable) technologies have received much attention due to ASIC and IC card applications. Moreover, with progress in microcomputer systems, high density EEPROM's have been in increasing demand. Of the three types of available EE technologies[1], (i.e., MNOS, floating-gate, and textured poly,) MNOS has the highest scalability because of its simple cell structure.

This paper closely evaluates shrunk MNOS devices, and describes new retention characteristic phenomena. From these results, an MNOS memory device is designed for Megabit EEPROM's.

2. Device Fabrication

N-channel Si-gate MNOS devices[2] with Si_3N_4 thicknesses(t_N) of 27.4, 23.8, and 19.8 nm, all with tunnel oxide thickness(t_{OX}) of approximately 1.6 nm, were fabricated for implementation in 64K bit, 256K bit, and 1M bit EEPROM's, respectively. The key steps for an MNOS memory device are as follows. 1) Tunnel oxide is formed at 850 ℃ by using a nitrogen diluted oxygen ambient. 2) Si_3N_4 film is deposited at about 790 ℃ under low pressure using mixed SiH_2Cl_2 and NH_3 gases. 3) High temperature H_2 annealing is performed at 900 ℃ after PSG deposition.

3. Shrunk MNOS Device Evaluation

Especially in MNOS, retention characteristics are the most important properties, including degradation during erase/write cycling. Experimental retention data for various programmed threshold voltages at 85 ℃ are shown in Fig. 1. To measure these data, devices are first saturated in the opposite threshold state by applying a long (300 ms) pulse to the gate of equal amplitude but of reverse polarity to the programming pulse. The upper group of the curves represents the written-state decay behavior, while the lower group represents that of the erased-state. $Vthi$ is the threshold voltage of the virgin memory device and $Vthm$ is that of the programmed

device. $Vthm$ varies with logarithmic decay after 1000 s and converges on $Vthi$.

The decay rate versus the threshold voltage difference between $Vthm$ and $Vthi$ is shown in Fig. 2. The decay rate is derived from the experimental threshold voltage decay 1000 s after programming. It should be noted that erased-state decay rates depend mainly on (proportional to) $Vthm$ only slightly on Si_3N_4 thickness(t_N). However, written-state decay rates are less dependent on $Vthm$, and decrease with t_N. These effects were demonstrated for the first time, implying that written-state charge distribution differs from that of the erased-state[3].

The insensible level and ten-year nonvolatility area are also indicated by arrows in Fig. 2. $Vthm - Vthi$ must be outside the shaded region in order to attain ten-year nonvolatility. The written-state charge decay determines the lower limit of $Vthm$, because only written-state $Vthm$ may be inside the shaded region.

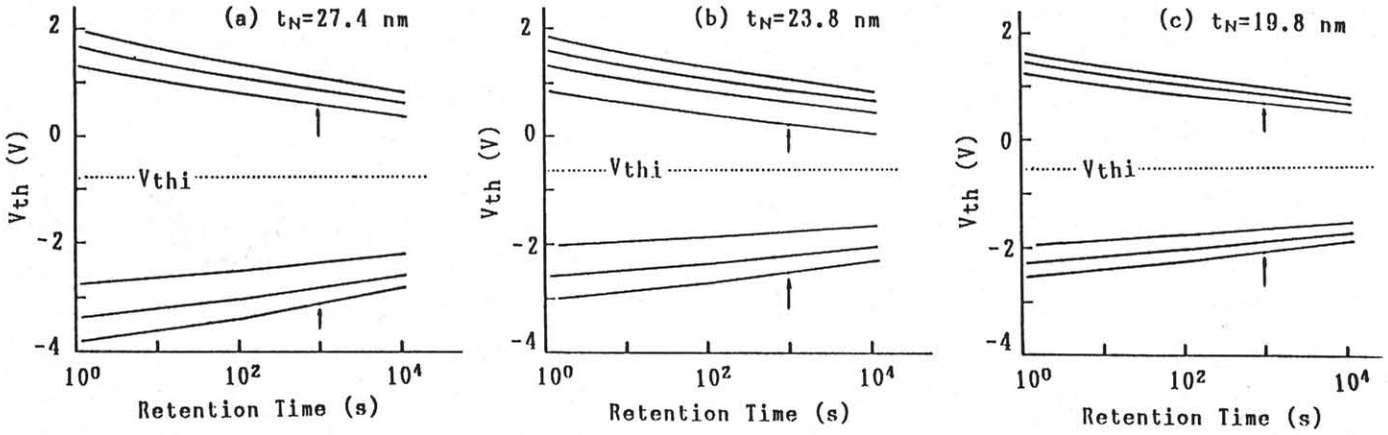

Fig. 1 Retention characteristics with various programmed threshold voltages at 85 ℃.

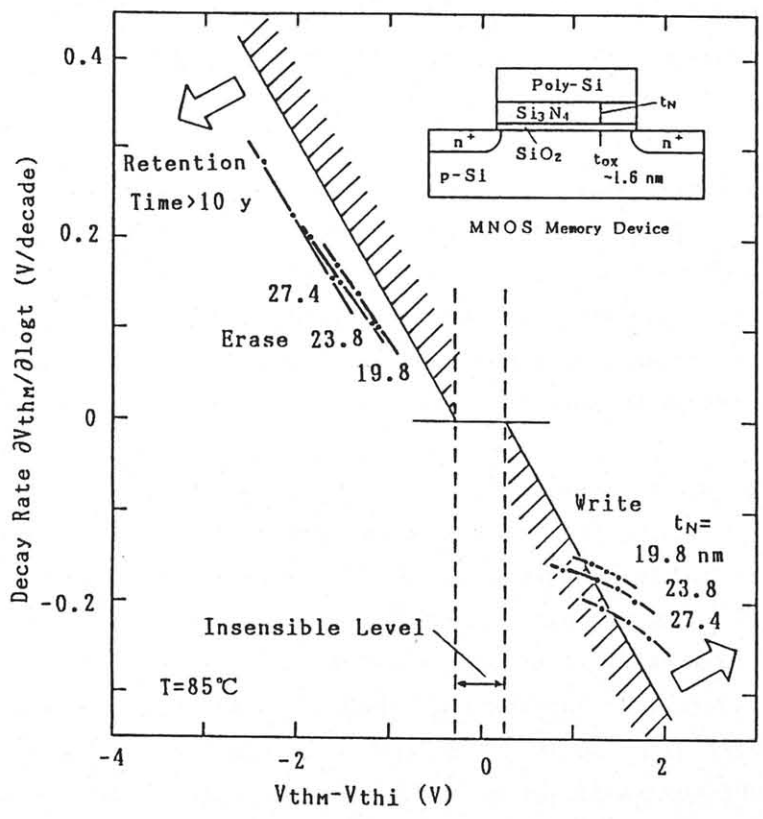

Fig. 2 Decay rate versus threshold voltage difference; decay rate behavior of the written-state differs from that of the erased-state.

Next, the effects of Si_3N_4 thickness (t_N) on endurance are investigated. The erase and write pulse widths are both 5 ms (maximum program time) and the spacing between alternating pulses is 200 μs. The pulse rise and fall times are 300 μs. As shown in Fig. 3, as long as the oxide electric field E_{OX} is constant, even if t_N is reduced, the memory window shift is smaller than in thicker t_N samples. The reduction of the transconductance coefficient β depends only slightly on t_N, as is shown in Fig. 4.

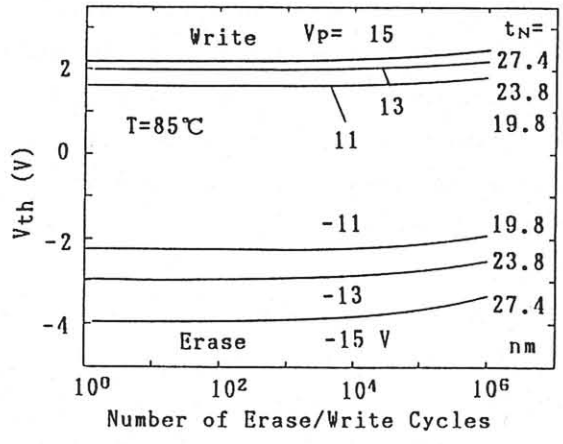

Fig. 3 Memory window versus erase/write cycles.

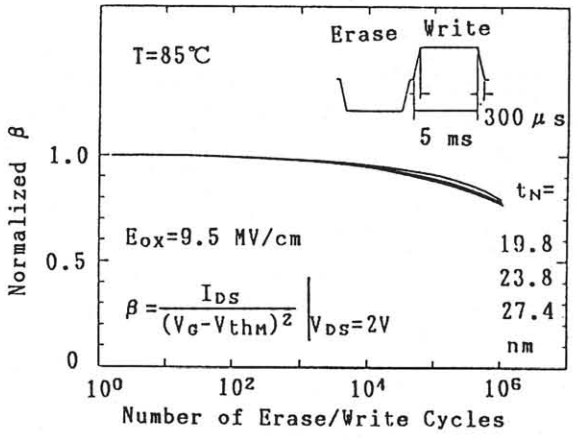

Fig. 4 Normalized transconductance coefficient versus erase/write cycles.

4. MNOS Design for Megabit EEPROM's

The margins of scaled-down MNOS devices are shown in Fig. 5. The lower limit of programming voltage Vp is determined by written-state retentivity, as shown in Fig. 2. It can be defined as the amplitude at a minimum write time 3 ms necessary to shift the threshold voltage to a required level. The Vp upper limit is determined by the $Vthm$ shift and by the increase in erased-state decay after the erase/write cycles. It varies with tunnel oxide thickness. For 1M bit EEPROM, Si_3N_4 thickness(t_N) is 20.0 ± 0.5 nm and Vp is 10.7 ± 0.5 V. The retention characteristics for 1M bit EEPROM memory devices are shown in Fig. 6. Ten-year nonvolatility after 10^4 erase/write cycles at 85 ℃ was confirmed.

64K bit test vehicles were evaluated by storing data at 200 ℃ after 10^5 erase/write cycles. No reliability problem occurred up to 1000 h, fully supporting our conclusion of ten-year nonvolatility at 85 ℃. Therefore, the feasibility of shrunk MNOS devices has been positively confirmed for use in LSI's.

Memory cell size can be less than 25 μm^2 if 0.8 μm design rules are used, as shown in Fig. 7. This is the smallest EEPROM

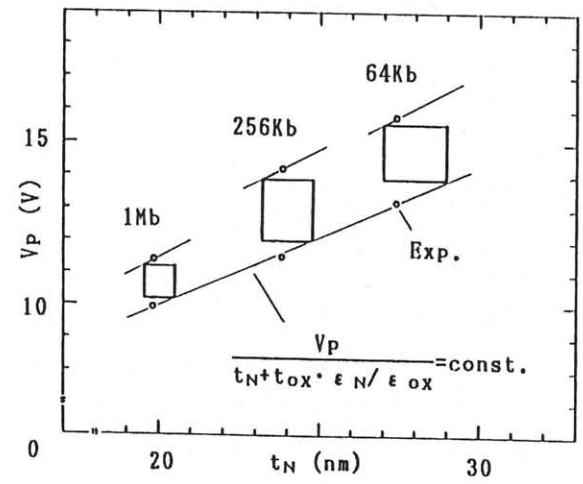

Fig. 5 Programming voltage Vp versus Si_3N_4 thickness for each density of EEPROM. Upper limit of Vp varies with tunnel oxide thickness.

cell size reported to date[4]. Memory cell consists of two transistors. A high-voltage structure MNOS memory transistor and a select transistor are connected in series. This configuration is the same as for the 64K bit EEPROM[2].

5. Conclusion

An MNOS memory device design for Megabit EEPROM's was developed. Shrunk MNOS devices were fabricated and investigated. The decay rate of the written-state decreases with Si_3N_4 thickness. It was shown that 1M bit MNOS EEPROM can be designed when t_N=20.0 nm and Vp=10.7 V. 64K bit test vehicles confirmed that shrunk MNOS devices can be used in LSI's. Memory cell size can be less than 25 μm^2. The MNOS device is a most promising candidate for Megabit EEPROM's.

Acknowledgment

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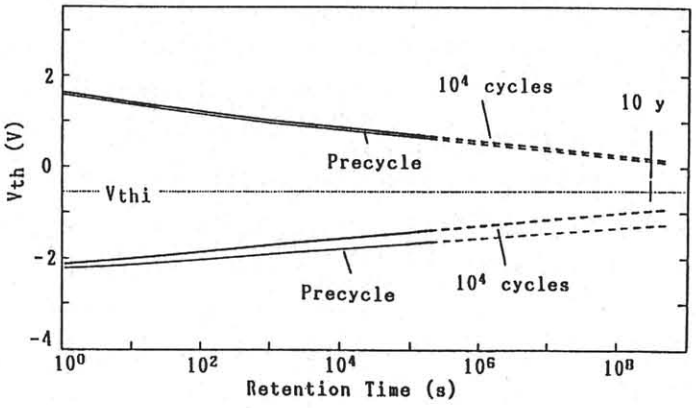

Fig. 6 Long term retentivity of MNOS memory device for 1M bit EEPROM at 85 ℃.

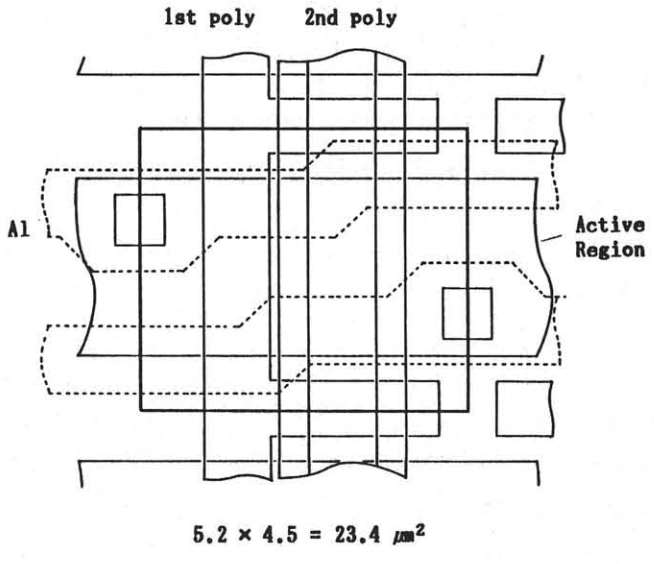

Fig. 7 Memory cell layout pattern with 0.8 μm design rules.