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Inter-Poly SiO_2/Si_3N_4 Capacitor Films 5nm Thick for Deep Submicron LSIs

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Thin SiO_2/Si_3N_4 composite films are examined to determine if they could be applied to megabit DRAMs. The electrical characteristics are found to be controlled mainly by the Si_3N_4 layer. In addition, direct tunneling current is found to be dominate when film thickness is reduced to 5nm or less. This tunneling current leads to practically infinite film life time, but adversely increases leakage current. This 5nm-thick composite film meets the data retention and reliability requirements of DRAM applications.

INTRODUCTION

Stacked and trench capacitors are the key to fabricating LSIs, especially megabit DRAMs. However, even in these structures, it is necessary to reduce film thickness in order to scale down future DRAMs or other devices.

Capacitor films are usually formed on poly-Si in stacked and trench capacitors [1][2]. Recent reports show that SiO_2/Si_3N_4 composite film is reliable even on poly-Si [3]. This paper presents findings that this composite film can be applied to deep submicron DRAMs. We found that the Time Dependent Dielectric Breakdown (TDDB) life time of the 5nm-thick composite film is sufficiently long for deep submicron DRAM use. However, the growing leakage current restricts the thinning limit when the film thickness (SiO_2 equivalent) is reduced to 5nm or less.

EXPERIMENTS

The samples investigated had poly-Si/dielectric/poly-Si structures. The lower poly-Si was deposited 300nm thick by LPCVD on selectively oxidized n-type Si substrates. After phosphorous diffusion utilizing $POCl_3$ source, the poly-Si was patterned by dry etching. Si_3N_4 films from 5nm to 18nm-thick were then formed and thermally oxidized in a steam ambient to provide the SiO_2/Si_3N_4 composite films. Finally, an upper poly-Si layer was deposited and patterned in the same manner as the lower poly-Si layer. The upper poly-Si layer covered the lower layer completely, thereby, making the capacitors free from gate-edge reliability problems. As the samples in this study have perimeter edges, the reliability results obtained should be applicable to actual DRAMs.

SiO_2 equivalent film thickness of the composite films, d_{eff}, was calculated from capacitance, adopting 3.82 as a relative dielectric constant. The electric field, E_{eff}, was normalized with the d_{eff}.

The d_{eff} of the samples investigated ranged from 3nm to 10nm.

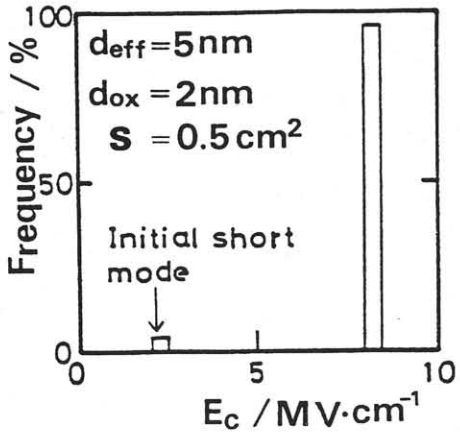

Fig.1 Distribution of critical fields for 5nm thick composite film.

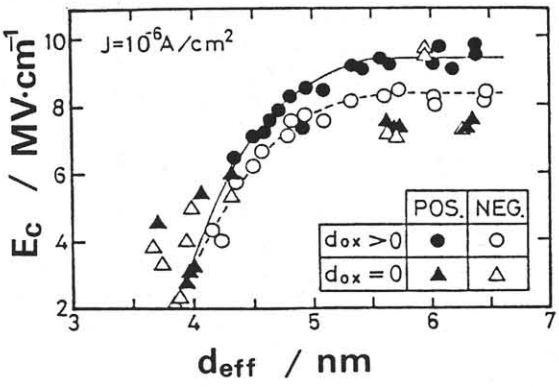

Fig.3 Critical field versus SiO_2 equivalent thickness.

RESULTS AND DISCUSSIONS

1. I-V CHARACTERISTICS

0.5cm² area capacitors were used in I-V measurement.

Fig. 1 shows the distribution of the critical fields, E_c, in positively biased capacitors with a composite film 5nm thick. Here, E_c is an electric field corresponding to a 10^{-6}A/cm² leakage current, and d_{ox} represents the top oxide thickness. The E_c distribution was very sharp and only a few capacitors (those in initial short mode) exhibited small E_c. The defect density of initial short mode, both in composite films (d_{ox}>0nm) and in Si_3N_4 films (d_{ox}=0nm), didn't increase and remained small (<0.2/cm²) even when d_{eff} was reduced to 3nm (see Fig. 2). This indicates that the thin Si_3N_4 films, formed on poly-Si, themselves have little pin-holes, which enables defect-free composite films. The critical fields, E_c, of the SiO_2/Si_3N_4 films are shown in Fig. 3. It is noteworthy that E_c decreased abruptly in the region where d_{eff}<5nm. The main concern in this study is the decrease in E_c for thinner films.

To investigate the origin of this decrease, the barrier height, ϕ_t, of the Poole-Frenkel process was calculated using the temperature dependence of the leakage current. Fig. 4 shows the ϕ_t of composite films (d_{ox}=2nm) and Si_3N_4 films (d_{ox}=0nm). For the higher electric fields, ϕ_t was nearly equal to the values of Si_3N_4 films reported so far [4][5] in each case where d_{ox}=0 and d_{ox}=2nm. On the other hand, it differed markedly from the reported value

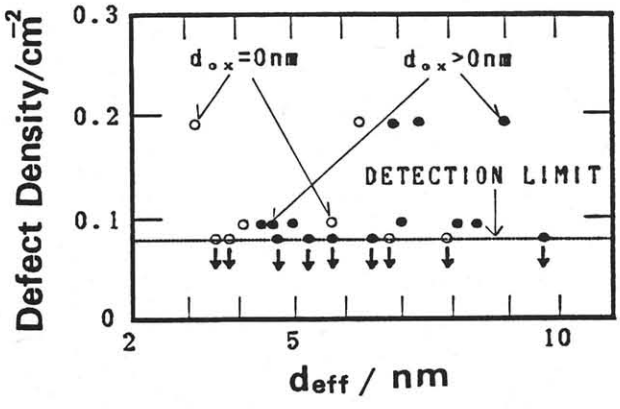

Fig.2 Defect density of initial short mode versus SiO_2 equivalent thickness.

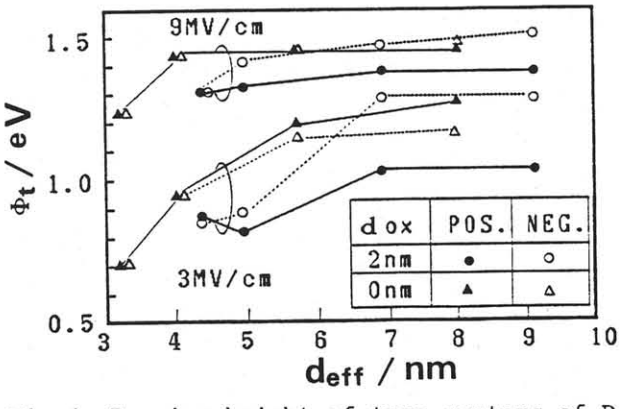

Fig.4 Barrier height of trap centers of P-F process versus SiO_2 equivalent thickness for different electric fields.

for the lower electric field, especially in the case of thin films.

These results suggest the following. The leakage current of thicker composite films is controlled by the Poole-Frenkel process in the constituent Si_3N_4 layer for the case of d_{ox}=2nm. This is reflected in the fact that the value of ϕ_t is equal to that of Si_3N_4 films. The decrease in ϕ_t for thinner composite films results from a newly dominating current component, which is possibly a direct tunneling current. Because of this tunneling current, E_c decreases as shown in Fig. 3.

2. TDDB CHARACTERISTICS

The time to breakdown, T_{bd}, was measured by stressing capacitors with a $10^{-6}cm^2$ area at a constant voltage. The result for a positive bias is shown in Fig. 5. The log(T_{bd}) increased linearly with a decrease in E_{eff}, and the slope of the log(T_{bd})-E_{eff} curve was larger in samples with smaller d_{eff} for each d_{ox}. As a result, reducing film thickness leads to a much longer lifetime under actual low fields. It is worth noting that T_{bd} in the case d_{ox}=2nm is longer than that in the case d_{ox}=0nm, as shown in Fig. 5. The electric field in the Si_3N_4 film is seemingly reduced by top oxide, resulting in a larger T_{bd}.

To further investigate the breakdown mechanism, the breakdown charge, Q_{bd}, was measured at the same time as T_{bd}. Q_{bd} increased with decreases in E_{eff}, in a way quite similar to that of T_{bd}, as can be seen in Fig. 6. This means that the current, which doesn't affect the dielectric breakdown, is more dominant for smaller E_{eff}. In addition, the slope of Q_{bd} vs. E_{eff} is larger in thinner composite or Si_3N_4 films. Both Fig. 5 and Fig. 6 show that the electric field dependence of T_{bd} and Q_{bd} are

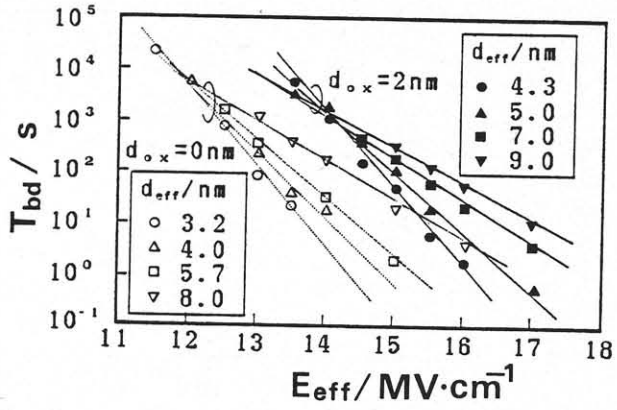

Fig.5 Time to breakdown versus electric field for positive bias.

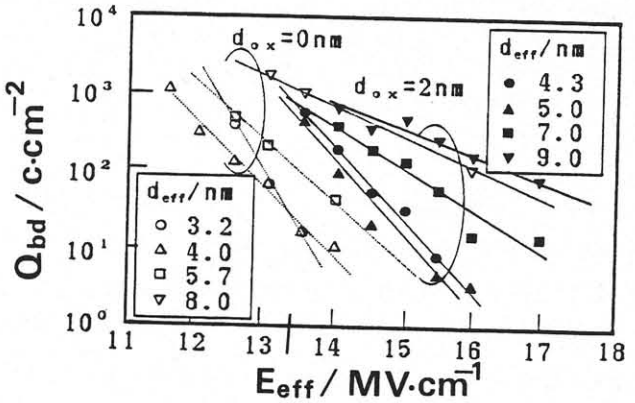

Fig.6 Breakdown charge versus electric field for positive bias.

not affected by d_{ox}, but by d_{eff} only. This result suggests that the dielectric breakdown of this composite film is triggered by the breakdown in the Si_3N_4 layer.

Fig. 7 shows the leakage current variation during the positive constant voltage stressing in composite films with different d_{eff}. It is clearly shown that the leakage current variations are smaller in thinner composite films. This indicates that only a slight degradation occurred in the films during stressing. This result also supports the dominance of the above-mentioned direct tunneling current in thinner composite films, because the tunneling current has little interaction with the films.

Thus, the following may be inferred from the above results. Thinner films and lower electric fields make the tunneling

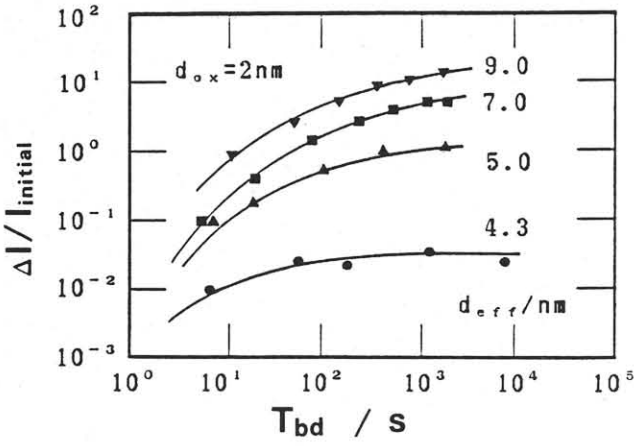

Fig.7 Leakage current variations in constant positive bias stressing versus time to breakdown.

$*\Delta I = I_{final} - I_{initial}$

current more dominant. This tunneling current interacts only slightly with Si_3N_4 film, resulting in a larger T_{bd} and Q_{bd}.

In previous work [3], it was reported that the dominant breakdown process in composite film is SiO_2 breakdown. In order to fabricate thinner composite films, typically 5nm thick, the top oxide thickness should be reduced to 2nm or less. In this case, the breakdown of composite films is controlled by the Si_3N_4 layer, as shown in this study. There are many works about SiO_2 breakdown mechanism [6][7][8]. However, few were reported about Si_3N_4 breakdown, which is waiting for further investigations.

CONCLUSION

Reducing SiO_2/Si_3N_4 film thickness to 5nm or less enhances the tunneling current through the film, resulting in a practically infinite lifetime. This sets us free from the conventional reliability constraint. Unfortunately, this tunneling current adversely increases leakage current at thicknesses below 5nm. Thus, the main concern now is to what extent leakage current can be allowed in developing capacitor films for deep submicron LSIs.

Nevertheless, this 5nm-thick composite film meets the data retention and reliability requirements of DRAM application.

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