Extended Abstracts of the 20th (1988 International) Conference on Solid State Devices and Materials, Tokyo, 1988, pp. 177-179

C-1-1

Effect of Annealing on the SOI Structure Formed by Large Dose Oxygen Implantation

Nan-Xiang Chen, Wei Miao, Zhong-Lie Wang, Chang Huang *

Inst. of Low Energy Nuclear Physics, Beijing
Normal University, PRC
* Shaanxi Lishan Micro-Electronics Institute,PRC

ABSTRACT: A silicon on insulator was formed by implanting I.8 X IO^{18} or 2 X IO^{18} oxygen cm^{-2} into crystalline silicon at 150 Kev. The effect of annealing on the microstructure were investigated by using RBS and cross-sectional TEM. The dependence of SOI structure on the annealed temperature were disscussed.

1. INTRODUCTION

Silicon on insulator structures have excellent potential for future use in radiation hardened Integrated Circuits(IC) and for high speed IC's. In the present study, the effect of post-implantation annealing on the SOI structure formed by implanted high dose O^+ were explored. The correlation of top Si layer, together with the properties of Si/SiO_2 interface, to annealed temperature were disscussed.

2. EXPERIMENTAL CONDITIONS

A dose of 1.8 X 10^{18} or 2 X $10^{18}/cm^2$ oxygen ions was implanted at 150 Kev into P-type silicon wafers of orientation(100) and resistivity 10-20Ωcm, the substrate temperature was held at 480°c during the implantation $^{1)}$. Microstructural analyses were performed by Rutherford backscattering/channeling analysis and cross-sectional TEM. The bulk oxygen concentration in top silicon layer was determined by the $^{16}O(\alpha,\alpha_0)^{16}O$

Table 1. Sample Histories

Wafer No.	Dose(O^+/cm^2)	ANNealing Condition	Experiments
S1	1.8 X 10^{18}	550 °c, 48h	RBS, SRM
S2	1.8 X 10^{18}	550 °c, 48h + 1400 °c, 10 Min	RBS, TEM, SRM
S3	2.0 X 10^{18}	1400 °c, 10 Min	RBS, $^{16}O(\alpha,\alpha_0)^{16}O$ Resonance
S4	2.0 X 10^{18}	1400 °c, 30 Min	RBS, TEM , SRM
S5	2.0 X 10^{18}	1400 °c, 60 Min	RBS, $^{16}O(\alpha,\alpha_0)^{16}O$ Resonance
S6	2.0 X 10^{18}	1250 °c, 2h	RBS, TEM, SRM
S7	2.0 X 10^{18}	1180 °c 6h	RBS, TEM
S8	2.0 X 10^{18}	1100 °c 8h	RBS, $^{16}O(\alpha,\alpha_0)^{16}O$ Resonance

resonance scattering. Details of the samples used was summarized in table 1.

3. EXPERIMENTAL RESULTS

After annealing, the RBS spectra from the sample S1, S2 and S5, in fig.1, clearly show the effect of annealing condition on the SOI structure. The random spectrum from the S5 shows the oxygen has redistributed completely to form an SOI structure with sharp interfaces of Si/SiO$_2$. The thickness of buried oxide layer basically reached the value which would be expe--cted from the implanted dose. It has been found that sample S1 has a thicker oxide layer than S5 although the implanted dose of S1 is smaller than of S5, as shown in fig.1(S1). The Si/SiO$_2$ interface of S1, although not sharp, could be considerably improved by annealing at 1400°c for 10 min, as shown in fig.1(S2).

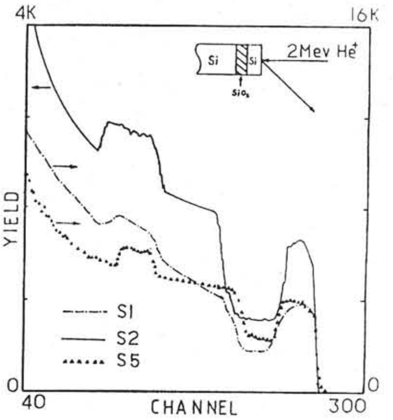


Fig.1 RBS SPectra of S1, S2, S5.

Fig.2 shows the RBS after annealing at 1400°c for different heat treatment time. As seen in fig.2, a stoichiometric buried layer with abrupt interface of Si/SiO$_2$ could be formed by a 30 min anneal at 1400 °c.

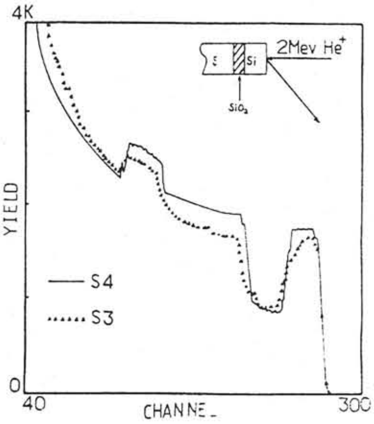


Fig.2 RBS Spectra of S4, S3.

Futher prolonging anneal time, though it could not result in any change in the oxide structure, is necessary to restore the damage in top silicon layer. Only by annealing at 1400 °c for 60 min, the entire top silicon layer become high quality single crystal, as shown in fig.3 where the surface minimum yield of top silicon layer is same as that of virginal single crystalline silicon wafer. The Hall mobility of the top silicon layer is 580 cm^2/ v·s. The cross sectional TEM of S5 shows that high quality SOI structure with no oxygen precitates and no transitional damage region has been obtained, the thickness of top silicon layer and buried oxide is 2000Å, and 3500 Å, respectively. CMOS devices with 1 m design rules and a 500 Å thick gate oxide

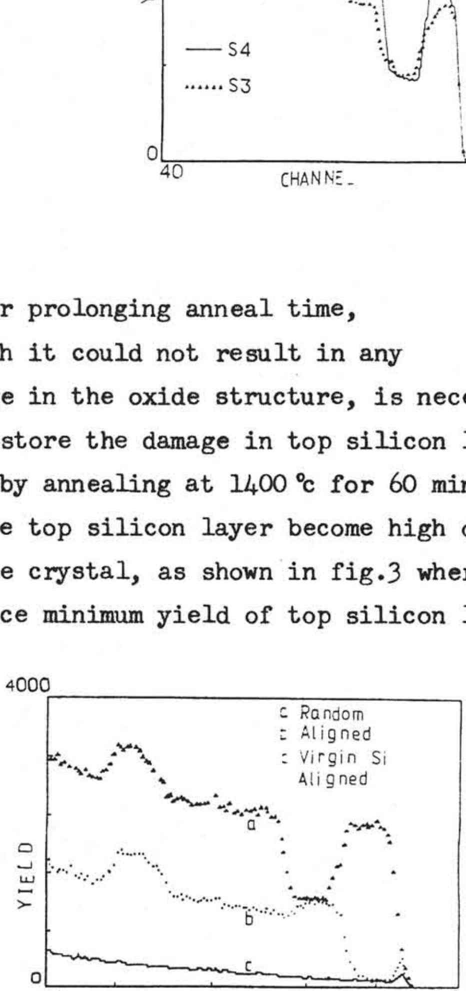


Fig.3 RBS and channeling spectra of S5

were successfully fabricated in an epitaxial silicon layer grown on the top Si.

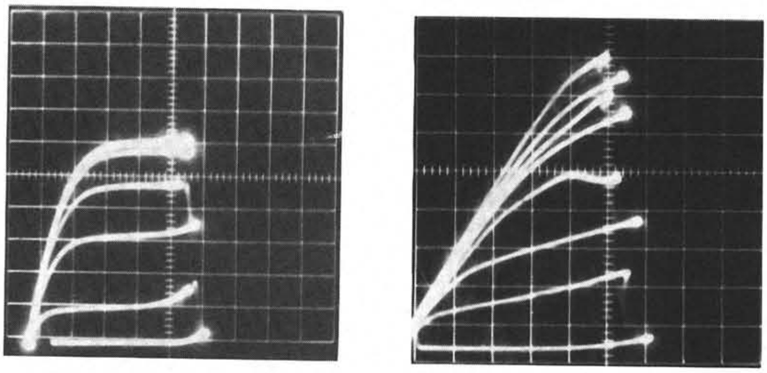
Fig.4a and 4b show the output characteristics of N- and P- channel buried oxide device, respectively. Both MOS transistor had W/L of 20/1 μm.

4. SUMMARY

In summary, annealing at 1400 °c has a profound effect on the crystallinity of top silicon layer and the properties of Si/SiO_2 interface. However , the oxygen concentration remained in the top silicon layer, which was measured by $^{16}O(\alpha,\alpha)^{16}O$ resonance scattering 2), was very high(10^{19}-10^{20} /cm^3). So long as these oxygen which far exceed oxygen's solid solution in silicon crystal exist, occuring of new precipitates is inevitable during sequential heat treatment at 1000 °c . In addition, the rich oxygen acts as electric donor, which makes the threshold voltage V_t of MOS device difficult to control. From the fact that a thicker oxide could be formed by 550°c anneal for 48h, which means that more oxygen was gettered from top silicon layer during forming of buried oxide, the two step anneal (550 °c+ 1400 °c) may be not only advantageous to the formation of top silicon layer with high crystallinity, but also to the elimination of oxygen precipitates.

REFERENCE

1). N.X.Chen et al, International Symposium on Application of Ion Beam Produced by Small Accelerators 1987,JiNan China,B-P-1
2). Z.L.Wang, Nucl Instr & Meth 211(1983)193



a. N- channel b. P- channel

Fig.4 Output characteristics of CMOS transistor (W/L : 20/ 1 . I_d : 0.01 mA/div, V_d: 1 v/div)