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Performance and Microstructural Analysis of 3D Circuits Fabricated in E-Beam Recrystallized SOI

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A dual electron beam technique has been used to make silicon-on-insulator (SOI) structures by zone melting recrystallization for three dimensional circuits. Stripes of device quality SOI material 40μm wide have been formed over underlying devices enabling a stacked CMOS structure to be fabricated. The vertically integrated circuit has a p-channel device in the SOI over an n-channel device in the bulk silicon.

1. Introduction

Three-dimensional (3D) integrated circuits based on silicon-on-insulator (SOI) technology offer many potential advantages over conventional integration in which only one layer of devices is used. The approach offers the possibility of vertical integration of optical detectors on top of signal processing or storage devices, high density memory configurations and the mixing of several different device technologies on the same chip (1, 2). The principal problem encountered in achieving 3D integration is in the preparation of material suitable for making further devices over previously fabricated devices in either the bulk material or a layer of SOI. The growth of the over layer must not damage the underlying devices and it must be device-worthy single-crystal silicon of thickness and planarity which is compatible with subsequent device design and fabrication processes such as lithography and etching. This paper describes development of a 3D process using SOI layers obtained by e-beam recrystallization.

2. The dual electron-beam recrystallization process

The silicon layers are formed by zone melting recrystallization in a dual electron beam thermal processing apparatus shown in Fig. 1(a) and schematically in Fig. 1(b) (3). The lower electron column produces a high power (2kW) electron beam which is rapidly scanned over the back surface of the wafer heating it uniformly to a background temperature of 950°C. The background temperature is held constant throughout liquid phase recrystallization, which takes less than 120s for a full 100mm wafer. The front surface is recrystallized in adjacent parallel stripes by a pseudoline 5 to 10mm long formed by scanning a 100μm spot with a 100kHz triangular wave form.

The wafer is prepared for the thermal process in the following manner. The devices fabricated in the bulk are laid out in parallel stripes with a width set by the need to have a regular array of seed windows for forming the SOI. A pitch of 43μm is used; the seed windows are about 5μ wide. A layer of silicon dioxide 1μm thick is deposited over the devices in the bulk and the seed windows are etched through to the bulk silicon. A layer of polycrystalline silicon 1μm thick is deposited over the wafer and capped, first with a layer of undoped oxide and a layer of phosphorus doped oxide. This

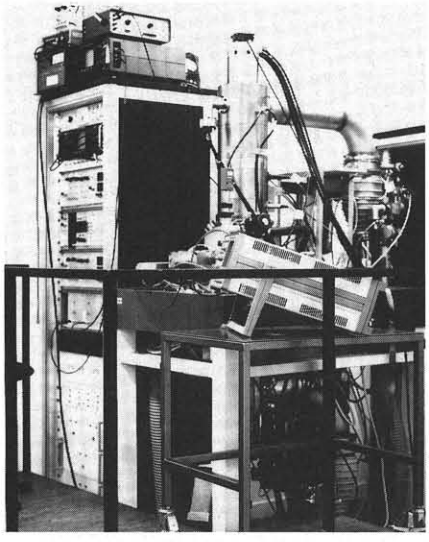

Fig. 1(a) Dual electron beam recrystallizer

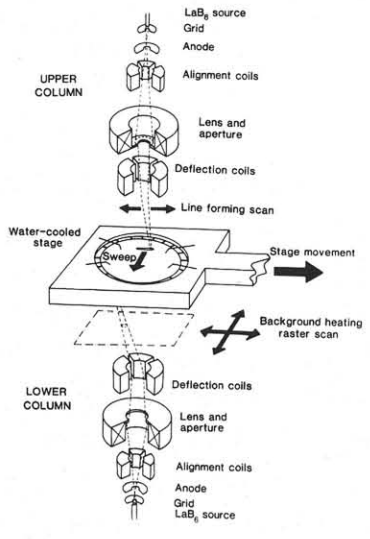

Fig. 1(b) Schematic diagram of dual e-beam recrystallizer

arrangement gives a flexible cap while preventing the doping in the upper layer from penetrating into the underlying polysilicon during recrystallization. The pseudoline is scanned parallel to the stripe direction over the full diameter of a 100mm wafer. The scan is aligned with respect to the chip so that end effects from the line fall in the scribe lanes and do not affect the active portions of the chip. A pseudoline power of around 40 W/mm at a scan speed of 45 cm/s melts the polysilicon and enough crystalline silicon in the seed windows to ensure seeded regrowth.

3. SOI Materials for 3D Integration

To be suitable for 3D circuit applications, the SOI layer must meet several practical requirements from the points of view of device design and performance, circuit layout and fabrication processes such as lithography. The silicon layer must have very few crystalline defects and it must have the desired thickness and crystal orientation. In dual e-beam recrystallization it is possible to form (100) oriented layers of 0.5 to 1μm thickness with the only defect being a line of crystalline faults running parallel to the seed windows where regrowth fronts from adjacent windows meet, as seen in Fig. 2. Devices and simple circuits formed in this material have given satisfactory performance (4). A spacing of 30 to 50μm between seed windows can be achieved which enables the layout of circuits of sufficient complexity to meet the needs of 3D applications. The planarity of the material can be improved by measures such as filling seed windows by selective epitaxially grown silicon in the windows to give a planar surface before deposition of polycrystalline silicon or by using a more rigid cap to limit bending during recrystallization. For 3D applications where the SOI is formed over previously fabricated devices surface, topography is particularly important. Processing conditions must be carefully controlled to obtain and maintain good material quality over a large areas where there are several changes in step height and to avoid melting vulnerable structures such as polysilicon gates. The thermal cycle must also be kept within strict bounds to prevent damage to underlying devices from excessive diffusion of dopants in previously implanted regions. An important requirement for multiple level 3D is that SOI layers should be seeded from a previously formed underlying SOI layer and Fig. 3 shows the cross-section of layers before the growth of an upper layer from an underlying SOI layer. With a dual e-beam recrystallizer and careful layer preparations material of satisfactory quality for the formation of SOI for 3D integrated devices has been processed.

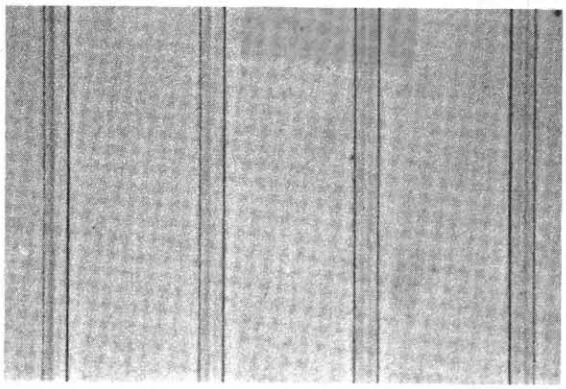

Fig. 2 Recrystallized SOI and seed window strips after Secco etching to reveal grain boundaries. The seed window pitch is 43 μm.

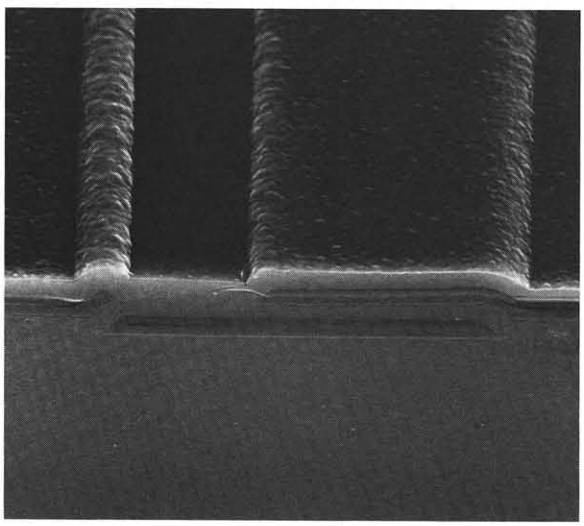

Fig. 3 Multiple layers of SOI formed by sequential seeding. Image width: 30 μm.

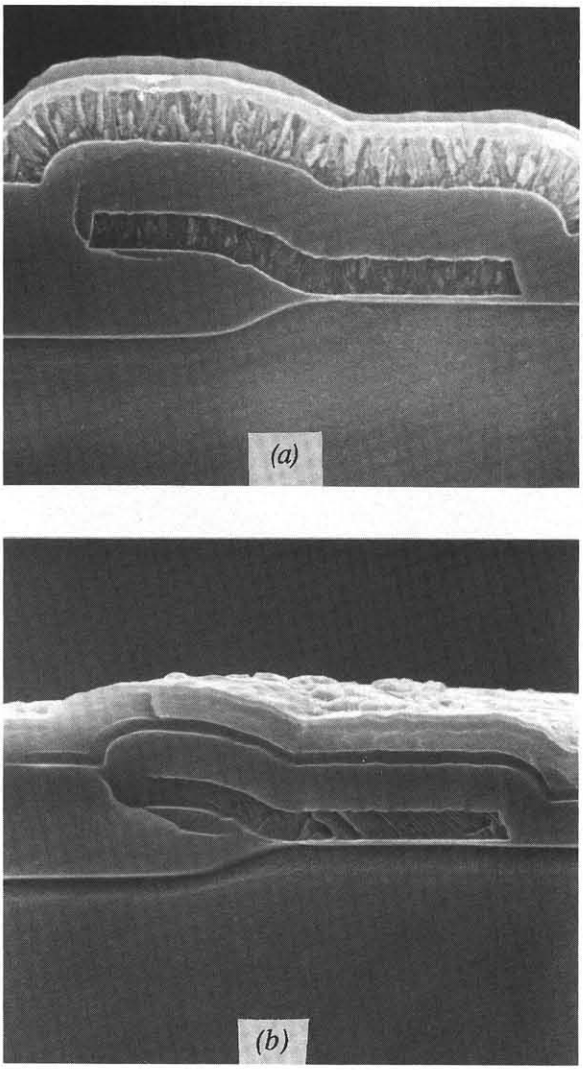

Fig. 4 Polysilicon gate of DMOS transistor
(a) before recrytallization of overlying SOI layer
(b) after recrystallization, showing melting of gate before melting in the bulk silicon.
The layer thicknesses are about 1 μm.

4. Device Assessment

Three types of devices have been studied in the research programme. The characteristics of devices in bulk silicon over which an SOI layer has been created have been measured to check for degradation (5). CMOS devices with as-drawn gates lengths ranging from 20μm to 1μm showed <0.1μm shortening in the electrical channel length after the recrystallization of an overlying unseeded layer. Breakdown voltage and off-state leakage did not change significantly from values exhibited by control wafers. Only small shifts in threshold voltage are predicted (6), since the thickness of the SOI layer was greater than the electron range so that very few electrons penetrate to the gate oxide, and the wafers are annealed further after recrystallization because the wafer stays at the background temperature for a few seconds longer.

The power window for recrystallization for single level SOI is normally taken to be between the power

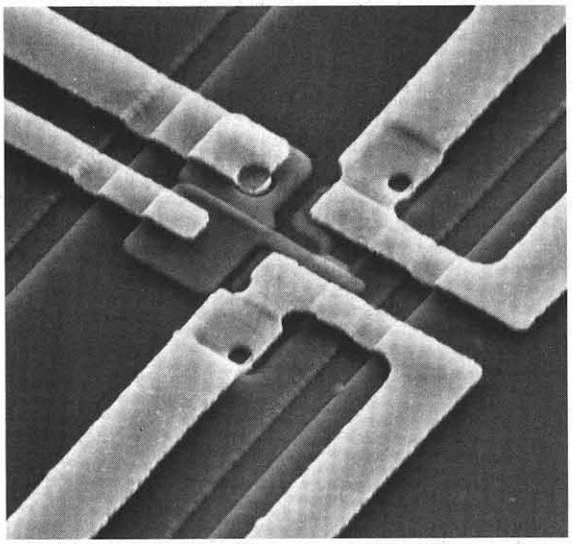

Fig. 5 Micrograph showing top view of stacked CMOS circuit.
The seed window pitch is 43 μm.

required to melt the seed to give seeded regrowth and the onset of melting under the isolating dielectric (7). The acceptable range for 3D compatible recrystallization was found to be less, as shown by studies on forming seeded SOI layers over bulk DMOS devices. The polysilicon gates of the DMOS devices are relatively well isolated thermally where they run over field oxide compared to gate oxide. Therefore, the gates melt before the bulk silicon as illustrated in the micrographs in Figs 4(a) and 4(b) showing the structure before and after recrystallization (12). For making 3-D circuits,the isolating dielectric cannot be a thermally grown oxide, but must be deposited. CMOS devices were fabricated in single layer SOI using either thermally grown or deposited oxide, and showed no substantial differences between the two dielectrics. Fully stacked CMOS devices with P-channel devices in the SOI layer and N-channel devices in the bulk were fabricated sucessfully by the National Microelectronics Research Centre (Cork, Ireland) in the material. The layout of the test structure, which performs as an inverter, is shown in Fig. 5.

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