Extended Abstracts of the 20th (1988 International) Conference on Solid State Devices and Materials, Tokyo, 1988, pp. 217-220

C-2-5

Interface State Generation Mechanism in MOSFET's during Substrate Hot Electron Injection

Naoki YASUDA, Hiroshi NAKAMURA, Kenji TANIGUCHI and Chihiro HAMAGUCHI
Department of Electronic Engineering, Osaka University
2-1, Yamada-Oka, Suita City, Osaka 565, Japan

Masakazu KAKUMU
Semiconductor Device Engineering Lab., Toshiba Corporation
1, Komukai Toshiba-cho, Kawasaki 210, Japan

Interface states created by substrate hot electron (SHE) injection are investigated in n-channel MOSFET's. It is found that g_m and S degradation show different dependence on stress gate voltage, which indicates the presence of two modes of interface states. The interface states at low gate oxide field are well explained by a bond breaking model. The electron capture cross section and the minimum formation energy of interface states are estimated to be 10^{-17} cm^2 and 3.5 eV, respectively.

1. INTRODUCTION

Interface states directly related to the degradation of MOSFET's have recently received a great attention as the VLSI circuit technology demands the use of submicron devices operating at higher electric fields. Although it is generally accepted that interface states are caused by the high energy carriers generated in the high field region, the generation mechanism is still poorly understood. The experiments performed in the normal operation of MOSFET's do not provide accessible information on the generation mechanism, because the generated interface states are localized in the drain region, which makes quantitative analysis difficult. In this study, the substrate hot electron (SHE) injection method[1] was used in order to generate interface states uniformly in the channel region. The dependence of interface state density on gate oxide field and electron energy was investigated.

2. EXPERIMENTAL

The samples used are n-channel MOSFET's in a (100) p-well with a gate area of 2.5×10^{-6} cm^2 as shown in Fig. 1. The gate oxide is 20 nm thick, and the p-well is 3 μm in depth with its doping density of 2×10^{16} cm^{-3}. Figure 2 shows the energy band diagram in the direction normal to the $Si\text{-}SiO_2$ interface. The p-well is reverse biased with respect to the source and drain. Forward bias is applied between the p-well and the n-substrate. Gate voltage

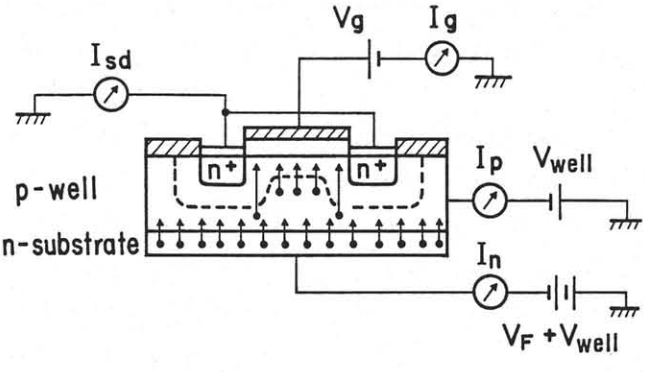

Fig. 1. Measurement circuit configuration for SHE injection.

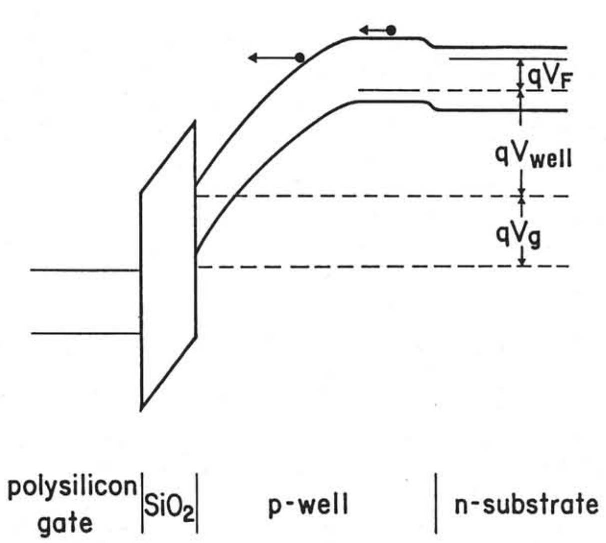

Fig. 2. Energy band diagram for injected electrons.

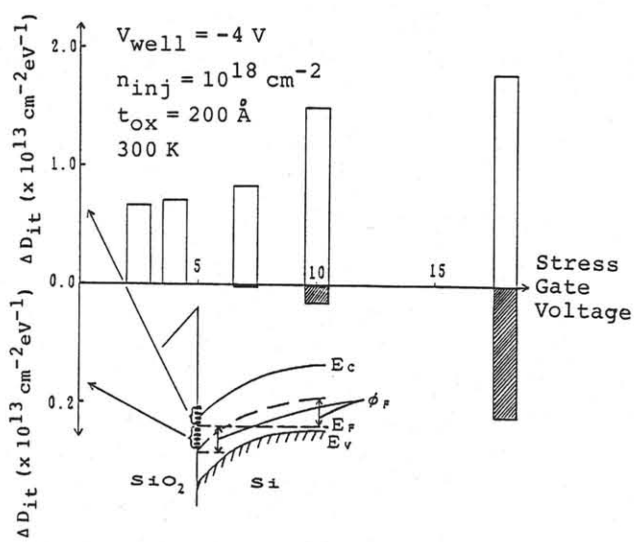

Fig. 3. Interface state density as a function of stress gate voltage. The p-well voltage was - 4.0 V, and the injected electron density through the gate oxide was 10^{18} cm^{-2}.

is kept positive enough to induce an inversion layer in the channel region in order to fix the surface potential. The electrons coming from the n-substrate diffuse through the p-well. Some of them arrive at the depletion layer edge and gain energy from the electric field in the depletion region during their drift towards the $Si\text{-}SiO_2$ interface. After reaching at the interface, some of the electrons with high energies are injected into the gate oxide, while most of them are collected in the source and drain. The SHE injection has advantage over Fowler-Nordheim injection, because SHE injection allows the independent control of the gate oxide field and the energy of injected carriers.

Interface state density was evaluated from the I_d-V_g characteristics of a MOSFET at drain voltage of 50 mV. The carrier injection and the I_d-V_g characterization were carried out using a HP-4145B parameter analyzer.

3. RESULTS AND DISCUSSION

Figure 3 shows the relation between stress gate voltage and generated interface state density in which the energy of injected electrons and the electron density through the gate oxide are kept constant. It should be noticed that the interface state density in strong inversion (mode A) slightly depends on the stress gate voltage, whereas that in the subthreshold region (mode B) shows strong dependence.

Figure 4 illustrates the two cases corresponding to low and high gate biases. If the gate voltage is as small as 2.5 V for a 20 nm gate oxide as shown in Fig. 4(a), the average electron energy at the gate electrode will be about 3.4 eV.[2] In this case, no hole trapping is expected, because the electrons do not gain energy enough to generate holes surmounting the $Si\text{-}SiO_2$ barrier. Therefore, interface state generation in low gate oxide field is attributed not to hole trapping but to the

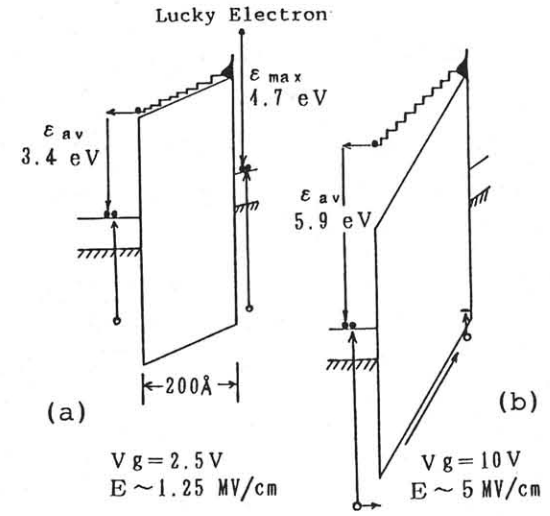

Fig. 4. Schematic illustration for two modes of interface state generation. The p-well voltage is - 4.0 V.

head-on collision of hot electrons with the strained bonds at the $Si\text{-}SiO_2$ interface. The fact that the interface state density of mode A shows slight dependence on the gate oxide field also supports this explanation.

On the contrary, at the stress gate voltage of 10 V as shown in Fig. 4(b), the electrons gain energy enough to generate surface plasmons[3] at the gate electrode. The holes created by the decay of surface plasmons will be injected into the gate oxide and subsequently be trapped at the $Si\text{-}SiO_2$ interface to generate interface states.

The discussions described above indicate that the interface state generation due to hot electrons (mode A: close to the conduction band edge) causes g_m degradation of MOSFET's, while the interface states generated by trapped holes (mode B: near the middle of the band gap) affect subthreshold characteristics.

Further investigation was made on the relation between the electron energy and the interface state density at low gate oxide field.

Figure 5 shows generated interface state density as a function of the p-well voltage. The injected electron density to the $Si\text{-}SiO_2$ interface is taken as a parameter in Fig. 5. The stress gate voltage was kept at 2.5 V. Negligible interface state generation below V_{well}=2.5 V indicates that interface state generation requires at least electron energy of 3.2 eV: minimum energy, $E_c=q(V_{well}+2\phi_F)$. An expression describing the generation of interface states at low gate oxide field is given by

$$N_{ss} = \int_{E_c}^{\infty} N_o\{1 - \exp(-\sigma n(E))\}dE, \quad (1)$$

where N_o is the density of breakable bonds with the formation energy of interface states between E and E+dE, σ is the electron capture cross section of the breakable bonds, n(E) is the density of the electrons with energies above E at the $Si\text{-}SiO_2$ interface, and E_c is the minimum formation energy of interface states. For

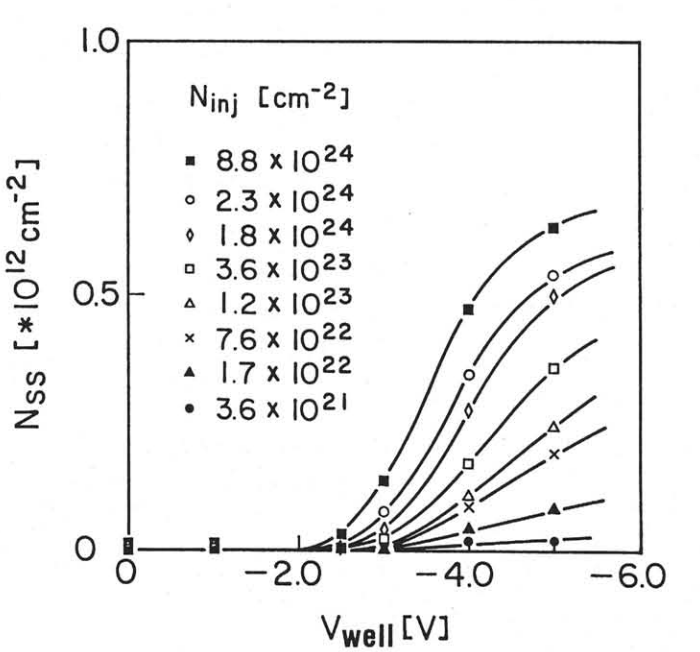

Fig. 5. Generated interface state density as a function of the p-well voltage. Stress gate voltage was 2.5 V.

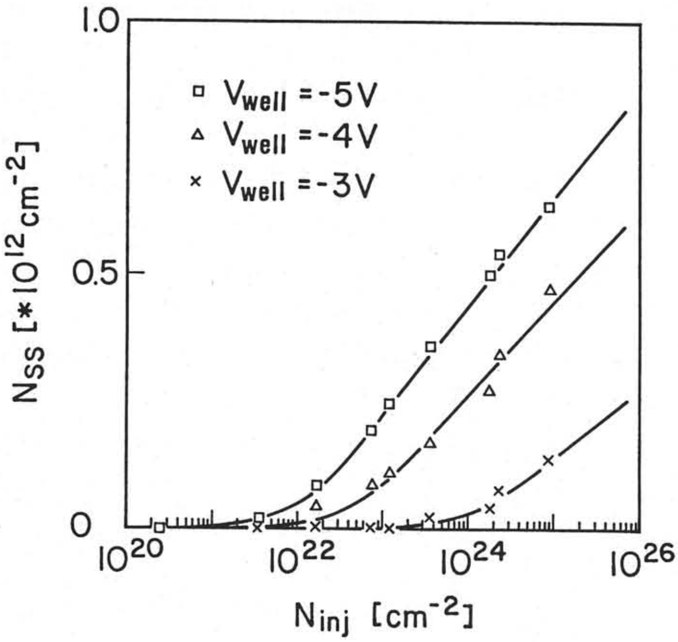

Fig. 6. Generated interface state density as a function of the electron density to the Si-SiO_2 interface. Squares, triangles and crosses are experimental results at stress gate voltage of 2.5 V, while the solid curves are calculated results.

simplicity, continuous and smooth distribution is assumed for the formation energy.

The measured interface state density as a function of the injected electron density to the Si-SiO_2 interface is shown in Fig. 6, with stress gate voltage kept at 2.5 V. The injected electron density to the interface is evaluated from

$$N_{inj} = J_{sd}\, t/q, \qquad (2)$$

where J_{sd} is the current density collected at the source and drain, and t is the duration of carrier injection.

The relations between N_{ss} and N_{inj} in Fig. 6 were fitted to the model by using three parameters, N_o, σ and E_c. The density of electrons with energies above E in Eq.(1) is expressed by

$$n(E) = J(E)\, t/q, \qquad (3)$$

where J(E) is the portion of the current density composed of the electrons with energies above E. J(E) is related to the measured gate current density as

$$J(E) = J_g \exp(-(E-q\phi)/k_B T_e), \qquad (4)$$

where ϕ is the barrier height of the Si-SiO_2 interface, k_B is Boltzmann constant, and T_e is the measured electron temperature. The solid curves presented in Fig. 6 is the calculated results with $\sigma = 10^{-17}$ cm^2, N_o = 3×10^{11} cm^{-2}eV^{-1} and E_c = 3.5 eV.

4. CONCLUSIONS

The interface states generated by hot electrons were investigated. It was found that there are two modes of interface states which are responsible for g_m degradation(mode A) and S degradation(mode B). The mode A was found to be well explained by a model based on the bond-breaking due to hot electrons. The electron capture cross section and the minimum formation energy of interface states were estimated to be 10^{-17} cm^2 and 3.5 eV, respectively.

REFERENCES

1) J. F. Verwey: J. Appl. Phys. 44 (1973) 2681.
2) S. D. Brorson, D. J. DiMaria, M. V. Fischetti, F. L. Pesavento, P. M. Solomon and D. W. Dong: J. Appl. Phys. 58 (1985) 1302.
3) M. V. Fischetti, Z. A. Weinberg and J. A. Calise: J. Appl. Phys. 57 (1985) 418.