

Physical Modeling of MOSFET Degradation Induced by High-Energy Hot-Carriers

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A physical model of hot-carrier induced MOSFET degradation is proposed. The model is based on an accurate gate current model and an extended mobility model. The injection process of high-energy carriers in avalanche region is successfully modeled. In addition, it is shown that the screening effect in the mobility model plays an important role in simulating the drain current and transconductance degradation. The present model allows the simulation of structure related hot-carrier induced MOSFET degradation.

Introduction

The hot-carrier induced device degradation has become a major problem in the scaling of MOSFET's. To model the hot-carrier effects, previous authors have considered the hot-carrier generation, emission process, carrier transport in the oxide, and oxide charge generation^{1),2)}. They have modeled the hot-carrier effects only caused by the channel hot-electrons.

In this work, a physical model of hot-carrier induced MOSFET degradation is proposed. The injection process of high-energy hot-carriers is accurately modeled. By comparing with the experimental data of gate currents, the effect of the high-energy hot-carrier injection is investigated in avalanche regions. In addition, the mobility model is extended including the screening effect of Coulomb scattering. It is shown that the screening effect plays an important role in modeling the drain current associated with device degradation.

Model of Device Degradation

The gate current model for device degradation simulations consists of calculating the carrier energy, the emission probability, the injection

current, and the carrier transport in the oxide. The carrier energy is calculated by using the effective carrier temperature model³⁾ to treat the steep gradients in the electric field. The emission probability is calculated by using the Richardson's emission model⁴⁾ which includes the Schottky-barrier lowering, the tunneling effect, and the scattering effect in silicon¹⁾. Also, the model considers the potential energy difference between the hot-carrier generation point and the injection point at the interface.

To calculate the injection current in the oxide, we propose the following injection model.

$$J_{inj}(x) = \begin{cases} J_{em}(\mathcal{E}) \exp\left(-\frac{x}{\lambda_{ox}}\right) - J_{em}(\mathcal{E} + \Delta\mathcal{E}) \exp\left(-\frac{x + \Delta x}{\lambda_{ox}}\right) & (\mathcal{E} > \mathcal{E}_B) \quad (1) \\ J_{em}(\mathcal{E}_B) \exp\left(-\frac{x}{\lambda_{ox}}\right) - J_{em}(\mathcal{E}_B) \exp\left(-\frac{x + \Delta x}{\lambda_{ox}}\right) & (\mathcal{E} \leq \mathcal{E}_B), \quad (2) \end{cases}$$

here $\mathcal{E}$ and $\mathcal{E}_B$ are the conduction band energy of the oxide at point x and at the interface, respectively. $J_{em}(\mathcal{E})$ represents the emission current density for the hot-carriers with energy more than $\mathcal{E}$ at the interface. λ_{ox} is the mean free path in the oxide. Fig.1 illustrates the hot-carrier injection into the oxide near the

drain region for $V_G < V_D$. Equation (1) allows the high-energy carrier injection against the electric field as shown in Fig.1. The injected carriers transport along the electric-field lines and some of them can reach the gate. The interface states are generated by the interaction between hole and electron injections¹⁾.

Moreover, the mobility model is extended from an earlier model⁵⁾ to calculate the drain current associated with device degradation. The normal electric field dependence of the mobility is written as,

$$\mu(E_{\perp}, N) = \frac{\mu(N)}{1 + \alpha p \mu(N) E_{\perp} (1 + \beta (E_{\perp})^{2/3})^{-1}} \quad (3)$$

here $\mu(N)$ is a bulk mobility reduced by the impurity scattering. $E_{\perp}$ is the electric field component normal to the current density. α and β are physical parameters. The parameter p is the surface scattering effects as follows,

$$p = p_0 + \sigma \cdot Nf \quad (4)$$

where p_0 represents the effects of surface roughness and surface phonon scattering. Nf is the interfacial charge density which is generated more than 10^{12}cm^{-2} by the hot-carriers. The scattering cross section σ is related to the carrier density in the inversion layer⁶⁾ in order to include the screening effect of Coulomb scattering.

Effect of High - Energy Hot - Carrier Injection

The present model is incorporated in the process / device simulator : SMART⁷⁾ and it is compared with the experimental data and the previous model. The previous injection model assumed that the hot-carrier energy is slightly larger than the barrier height. Therefore, no carriers can be injected into the oxide against the electric field even if the carriers have the high-energy.

The effect of high-energy hot-carrier injection is investigated by measuring and simulating the gate current-voltage characteristics for submicrometer MOSFET's in Fig. 2 (a) and (b). The experimental results indicate the shoulder shape of the gate current caused by the

injection of the avalanche hot-carriers⁸⁾ and it becomes more considerable as the MOSFET's are scaled down to submicrometer dimensions. At the bias condition of $V_G < V_D$, the present model simulates the shoulder shape of the gate current, while the result using the previous model decreases steeply as the gate voltage decreases. To clarify this difference, the injection process is investigated in detail for a $0.7\text{ }\mu\text{m}$ MOSFET. Fig. 3 (a) and (b) show the injection current density at the interface and the gate current density when $V_G = 5.5$ and 3.5 V , respectively. The electric field lines are also shown in Fig. 3 (a) and (b). At the right side of the critical field line A - A', the electric field lines return to the silicon. This means that at the right side of the point A, the gate current density consists of only high-energy hot-carriers injected against the electric field. In Fig. 3 (a), there is relatively little difference between the two models in the gate current density. As the gate voltage decreases, the high-energy carrier injection becomes a major part of the gate current density as shown in Fig. 3 (b) because the critical field line A - A' shifts to the channel side. As a result, the present model can simulate the shoulder shape of the gate current in the avalanche region while the gate current using the previous injection model decreases steeply with the decrease of the gate voltage. As the gate length is scaled down, the carrier energy becomes higher and the carrier injection against the electric field is enhanced. Therefore, the present model can successfully predict the gate length dependence of the shoulder shape of the gate current.

Results in Submicrometer MOSFET

Using the present injection model, the device degradation is simulated before and after stressing at the avalanche region for conventional n-channel MOSFET. The density and distribution of the trapped carriers and the generated interface states are calculated

from the injection current density. To clarify the screening effect on the mobility reduction, the present model is compared with the experimental data and the non-screening mobility model. The non-screening mobility model assumed that the scattering cross section σ in eq. (4) is constant. The drain current degradations are plotted in Fig. 4 using the two models. The degradations are normalized by the value of the drain current degradation at $V_G=1.2$ V. As the gate voltage is increased, the difference between the two models increases. In the present model, as the drain current increases, the screening effect moderates the mobility reduction caused by the interfacial charges. In non-screening mobility model, the mobility reduction is induced even in high gate voltage region. This induces the discrepancy of the drain current simulated by the non-screening mobility model. The present mobility model agrees well with experimental data even in high gate voltage regions. In addition, the transconductance degradation at each gate voltage is calculated in Fig. 5. As the gate voltage is increased, G_m degradation using the present mobility model is suppressed. This is consistent with the experimental data. These characteristics are inherent in the conventional MOSFET⁹⁾. In the case of non-screening mobility model, the result gives a parallel shift of G_m which is the inherent characteristics of LDD MOSFET⁹⁾. The screening effect of Coulomb scattering plays an important role in predicting the structure related device degradation.

Conclusion

The model of hot-carrier induced MOSFET degradation have been proposed, which is based on the accurate gate current model and the mobility model including the screening effect of Coulomb scattering. For accurately modeling the gate current, the injection process of high-energy hot-carriers in avalanche region has been successfully modeled. In

addition, it has been shown that the screening effect in the mobility model plays an important role in simulating the drain current degradation induced by the hot-carriers. The present model allows the simulation of the structure related hot-carrier induced MOSFET degradation.

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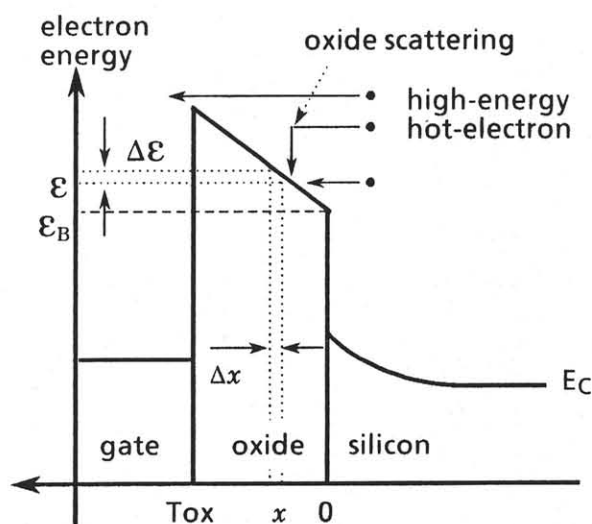


Fig.1 Energy-band diagram near the drain for $V_G < V_D$.

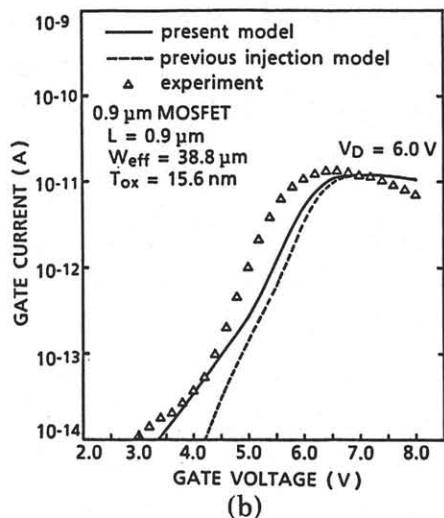
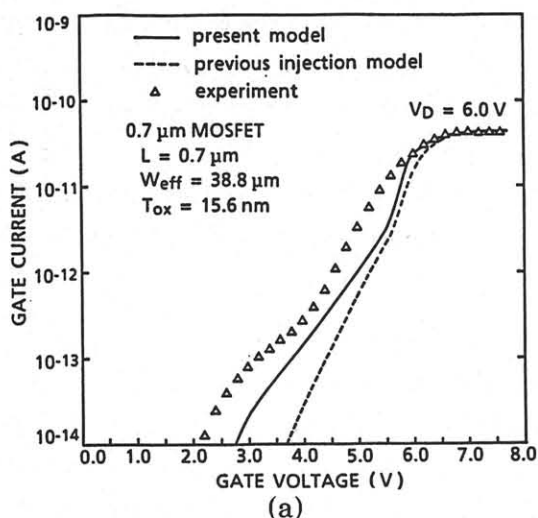


Fig.2 Gate current versus gate voltage at a drain voltage of 6.0V. In two test devices, gate oxide thickness is 15.6 nm and effective channel width is 38.8 μm . (a) The test device has a gate length of 0.7 μm . (b) The test device has a gate length of 0.9 μm .

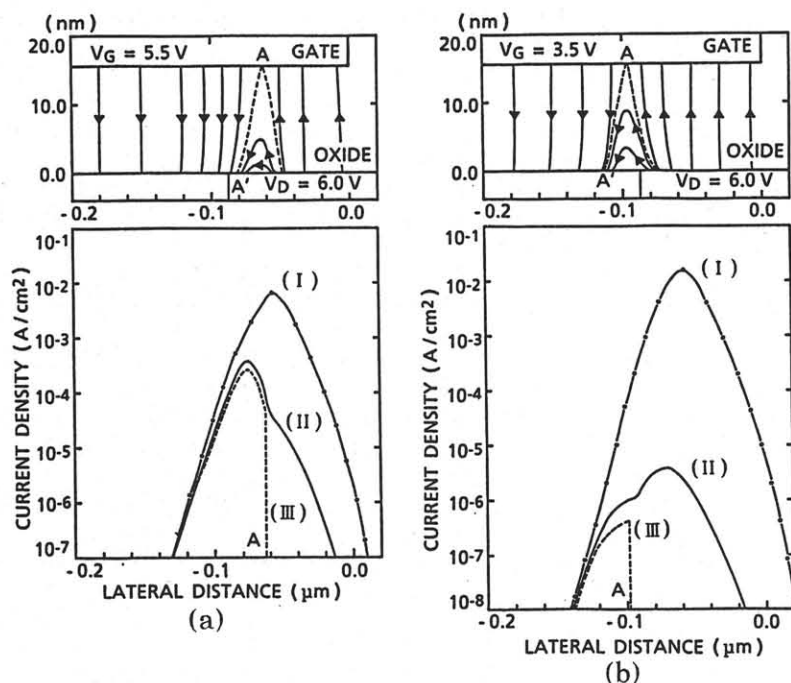


Fig.3 Lateral distributions of injection current density at the interface (I), gate current density calculated by the present model (II), and gate current density calculated by the previous injection model (III) for a 0.7 μm MOSFET. The electric field lines in the oxide are also illustrated. (a) $V_G = 5.5\text{V}$ (b) $V_G = 3.5\text{V}$

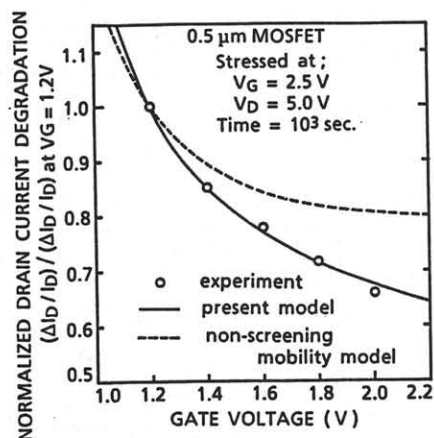


Fig.4 Normalized drain current degradation versus gate voltage. The test device has a gate length of 0.5 μm , a effective channel width of 8.8 μm , and a gate oxide thickness of 10.2 nm.

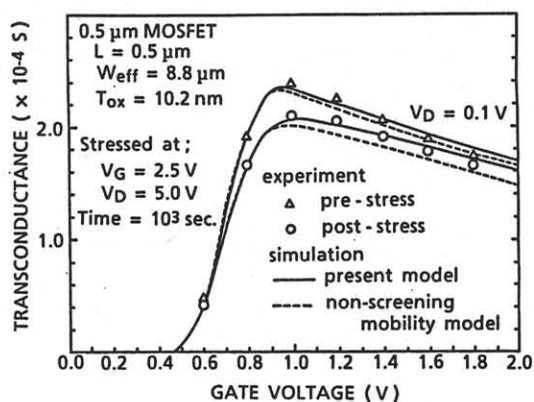


Fig.5 Transconductance degradation versus gate voltage. The transconductance is measured at $V_D = 0.1\text{V}$. The test device is similar to that in Fig.4.