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Effects of PAs_xN_y Deposition Conditions on the Characteristics of $In_{0.53}Ga_{0.47}As$ Metal-insulator-Semiconductor Field Effect Transistors

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Effects of deposition temperature of PAs_xN_y film and Cd concentration in the substrate on the electrical characteristics of $In_{0.53}Ga_{0.47}As$ metal-insulator-semiconductor field effect transistors were investigated. It was found that effective mobility of electrons increases with the decrease of the deposition temperature of film and of Cd concentration in the substrate, and has exceeded 2000 cm^2/Vs at room temperature. The dependence of threshold voltage on film deposition temperature was studied and attributed to the change of interface charge. The drain current drift of MISFETs was suppressed within 10% of the initial value in 10^3 s by using vapor phase etching before film deposition.

1. Introduction

Characteristics of III-V ternary or multi-ternary metal-insulator-semiconductor field effect transistors (MISFETs) are much affected by their gate insulator-substrate interface properties[1-3] and their substrate properties.[4]

We have already demonstrated the feasibility of the inversion type $In_{0.53}Ga_{0.47}As$ (InGaAs) MISFETs using PAs_xN_y(PAsN) film as the gate insulator, which has excellent interface property, in conjunction with vapor phase etching technique and in-situ deposition of gate insulator.[5]

In this paper, the effects of deposition temperature of PAsN film and Cd concentration in the substrate on electrical characteristics of InGaAs MISFETs will be presented.

2. Experimental

The InGaAs substrates used in this experiment were prepared by liquid phase epitaxy on InP wafers. The n^- wafers for MIS diodes were undoped and the carrier concentration and Hall mobility at room temperature were $2x10^{16}$ cm^{-3} and about 9000 cm^2/Vs, respectively. The p-type wafers for n-channel MISFETs were doped with Cd and a carrier concentration was ranged from $7x10^{15}$ to $8x10^{16}$ cm^{-3}.

PAsN films were deposited by chemical-vapor-deposition (CVD) system using PCl_3, $AsCl_3$ and NH_3 as reagent gases as reported previously[5]. Vapor phase etching was carried out using $AsCl_3$ gas before the PAsN film deposition to remove natural oxide from the InGaAs surface.

The MISFETs were of ring gate type. The inner and outer diameters are 200 μm and 400 μm, respectively.

3. Properties of interface between PAsN film and the InGaAs substrate

The density of interface trap states, Nss, evaluated by using Terman's method in the energy gap of InGaAs for various vapor etching and PAsN deposition temperatures is shown in Fig.1. The minimum Nss which is located at about 0.15 eV above the midgap of InGaAs decreases with reducing the vapor etching and the deposition temperature. The minimum Nss for PAsN/InGaAs system was about

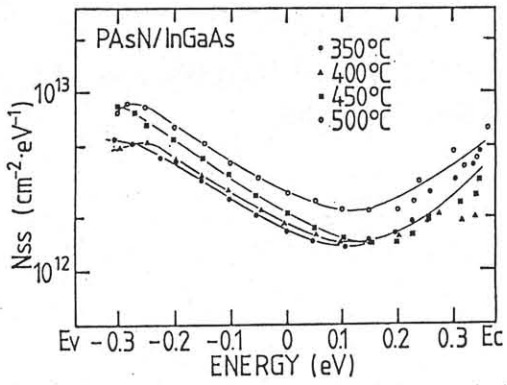

Fig.1 The density of interface trap states for various vapor etching and PAsN deposition temperature.

$1x10^{12}$ cm^{-2}, which was obtained by the vapor etching and the deposition temperature at 350 °C.

4.MISFETs' characteristics

A.Electron mobility

The effective mobility of electron, μ_{eff}, in the channel of InGaAs MISFETs calculated from the linear region of the current-voltage characteristic as a function of the etching and the PAsN deposition temperature is shown in Fig.2. The μ_{eff} decreases with the rise of the etching and the deposition temperature and the value of μ_{eff} in the MISFETs fabricated by the deposition temperature of 350 °C is about a factor of 4 larger than that by the deposition temperature of 500 °C.

The difference of Nss near the conduction band edge between the MIS diode fabricated by the deposition temperature of 500 °C and that of 350 °C is $3x10^{12}$ cm^{-2} eV^{-1}, as shown in Fig.1. This means that the difference of the number of trapped electrons is about $3x10^{11}$ cm^{-2} for the surface potential of 0.1 eV. On the other hand, induced electron density is about $8\text{-}10x10^{11}$ cm^{-2} for the linear region used to determine μ_{eff}. In consequence the difference of μ_{eff} is not completely attributed to the trapping of induced electrons, but more process induced scattering potential centers for electrons is possible for the former because of the higher deposition temperature .

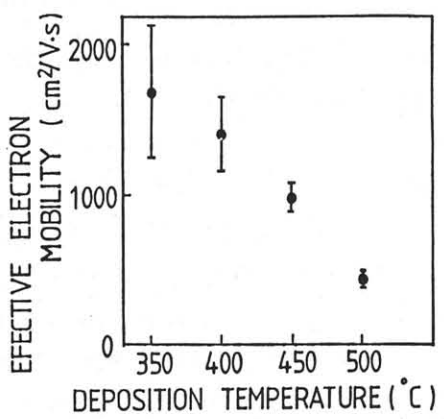

Fig.2 Effective mobility of electrons as a function of the vapor etching and PAsN deposition temperature.

Figure 3 shows μ_{eff} in the channel of MISFETs as a function of Cd mole fraction in the melt from which the ingot for the substrate was grown. It can be seen that the μ_{eff} decreases with Cd mole fraction and μ_{eff} for Cd mole fraction of $1.4x10^{-4}$ is 2000 cm^2/Vs which is a factor of 4 smaller than the bulk value. However the magnitude of μ_{eff} are slightly different between two runs and μ_{eff} does not only depend on the Cd mole fraction, but also the distribution of Cd in the substrate and/or another unintentionally doped impurities.

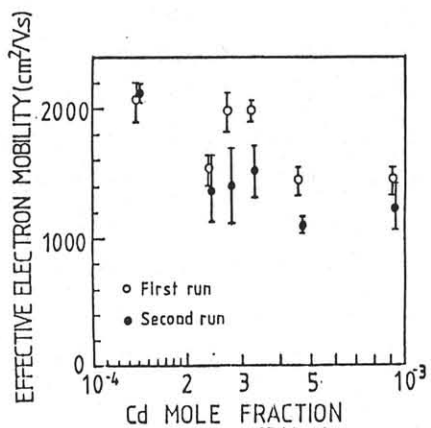

Fig.3 Effective mobility of electron as a function of Cd mole fraction in the melt from which the ingot for the substrate was grown.

Effective electron mobility which was measured as a function of induced electron density, Ns, on the substrate with a parameter of the measuring temperature for the

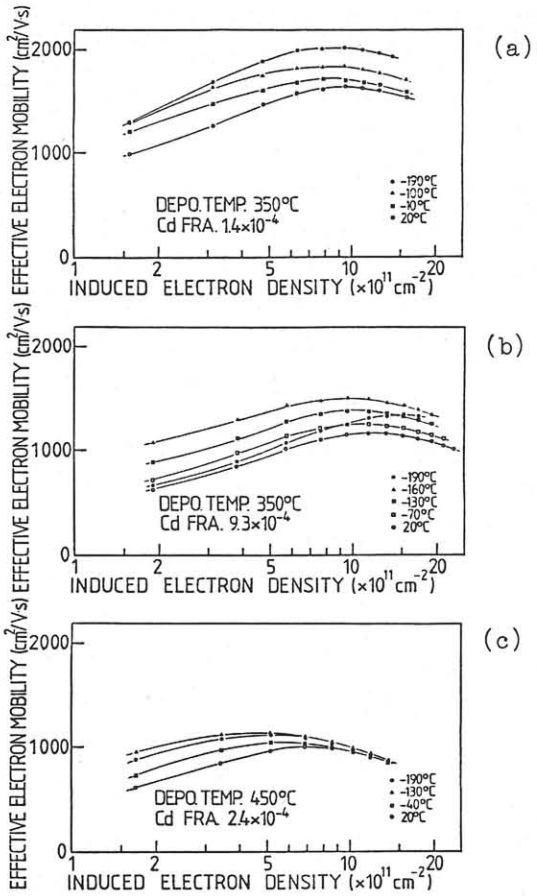

Fig.4 Effective mobility of electron as a function of N_s on the substrate with a parameter of the measuring temperature.

MISFETs prepared on the substrate with different Cd concentration is shown in Fig.4. The μ_{eff}, shown in Fig.4(a), monotonically decrease with the rise of temperature, but the μ_{eff}, shown in Fig.4(b), has a peak at -140 °C. The scattering mechanism for μ_{eff} which has positive dependence on Ns at low temperature is considered to be due to ionized impurity. This result also supports that doped Cd affects effective mobility of electron as major scattering centers. Furthermore, μ_{eff} of MISFETs whose etching and deposition temperature is 450°C, which is shown in Fig.4(c), is higher for Ns region of 5-7x10^{11} cm $^{-2}$ for any temperature among μ_{eff} shown in Fig.4(a), (b) and (c) and shows more rapid fall-off above Ns of 7x10^{11} cm^{-2} compared to the μ_{eff} shown in Fig.4(a) and (b). The scattering mechanisms for μ_{eff} which has such a negative dependence on Ns at high Ns region are thought to be polar optical phonon scattering ,surface roughness scattering and localized potential like delta-function-like scattering.[6] In fact, as poor surface morphology was observed after vapor etching at high temperature, surface roughness and/or localized potential due to defects induced at high processing temperature are thought to be most responsible for the reduction of μ_{eff} in the surface layer of MISFETs.

B.Threshold voltage

Figures 5 and 6 show the threshold voltage, V_{th}, as a function of vapor etching and PAsN deposition temperature, and Cd mole fraction in the melt, respectively. The V_{th} decreases with a rise of vapor etching and PAsN deposition temperature and increases with doped Cd mole fraction in the melt. The difference of the threshold voltage, V_{th}, for the FETs fabricated by the deposition

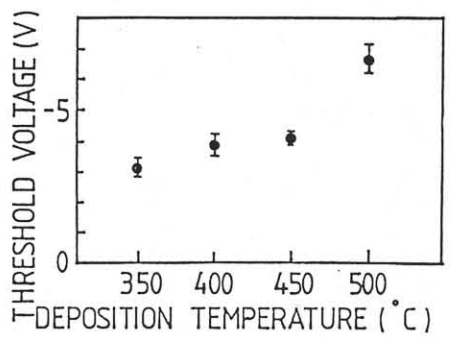

Fig.5 Threshold voltage as a function of vapor etching and PAsN deposition temperature.

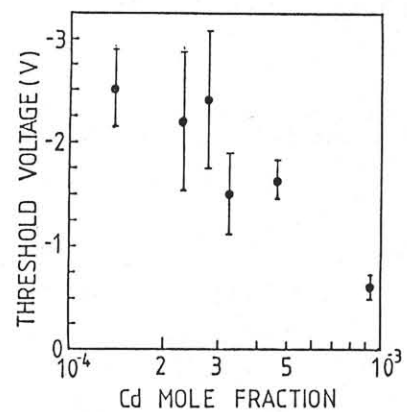

Fig.6 Threshold voltage as a function of Cd mole fraction in the melt.

temperature between 350 °C and 500 °C is about 3.7 V as shown in Fig.5 and this is almost consistent with the change of Qss/q which is estimated to 2×10^{12} cm^{-2}. The variation of V_{th} for the different Cd mole fraction as shown in Fig.6 is also understood due to the change of ϕ_F and N_A.

C.Drain current drift

The drain current drift for MIS FETs fabricated by various vapor etching and PAsN deposition temperature is shown in Fig.7, where the drain current is normalized with respect to the current measured 0.5 second after the gate bias application. The drain current drift is almost independent of the PAsN deposition temperature and the value was 10 % of the initial value, which shows a increasing type drift. While the physical origin of the drain current drift is still unclear, the vapor phase etching, which must be effective for the temperature range from 350°C to 500°C, reduces the current drift in the MIS FETs.

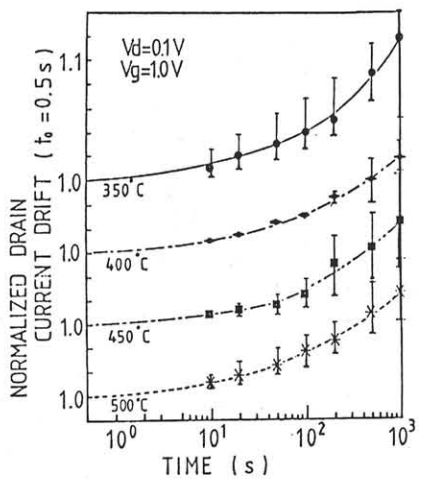

Fig.7 The drain current drift for the various vapor etching and PAsN deposition temperature.

5.Conclusions

Effective mobility of electrons in the channel was found to decrease with the rise of the deposition temperature and the increase of Cd concentration in the substrate, due to the increase of process induced defects and Coulomb scattering centers, respectively. The variation of threshold voltage was concluded to be understood by the change of the density of interface trap states and the surface Fermi energy. Furthermore the drain current drift was found to be suppressed by vapor phase etching before the PAs_xN_y deposition.

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