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MESFETs on GaAs/Fluoride/Si Structures

Kazuo TSUTSUI, Tanemasa ASANO, Hiroshi ISHIWARA and Seijro FURUKAWA

Dept. of Applied Electronics, Graduate School of Science and Engineering
Tokyo Institute of Technology
4259 Nagatsuda, Midori-ku Yokohama 227 JAPAN

MESFET's were fabricated on single domain GaAs/fluoride/Si structures which were grown by MBE. The single domain GaAs layers were obtained by introduction of a double-fluoride layer composed of $(Ca,Sr)F_2$ and CaF_2, as well as use of off-oriented Si(100) or Si(511) substrates. gm=12mS/mm and $K=0.8mA/V^2$ were obtained for an FET with Lg=7μm and Wg=140μm.

1. Introduction

GaAs-on-Si has been actively investigated, however, there are still problems of crystalline defects in GaAs layer, which results from mismatches of lattice parameters and thermal expansion coefficients between GaAs and Si. These problems may be solved by use of a $GaAs/Ca_xSr_{1-x}F_2/Si$ structure, where a crystalline insulator layer is inserted between GaAs and Si as a buffer layer. The lattice constant of $Ca_xSr_{1-x}F_2$ can be varied continuously by the mixing ratio between SrF_2 and CaF_2 and closely matched to both GaAs(x=0.43) and Si(x=1.0). Since the thermal expansion coefficient of $Ca_xSr_{1-x}F_2$($18-19\times10^{-6}$/deg.) is much larger than that of GaAs, thermal strain in the GaAs layer which is produced by the smaller expansion coefficient of Si may be relaxed at RT by insertion of the fluoride layer. Moreover, perfect electrical isolation between GaAs and Si is attractive for applications such as very high-speed IC's, OEIC's, and 3-D IC's.

From the viewpoints of device applications, growth on (100) face is desirable. (100) oriented GaAs growth on $(Ca,Sr)F_2$ has been investigated in the structure of $GaAs/(Ca,Sr)F_2/GaAs(100)$[1,2]. Optimum conditions to grow GaAs layers with good electrical characteristics on the fluoride have been studied and device fabrications have successfully been demonstrated in this structure [3,4]. On the other hand, studies on GaAs-on-fluoride structures using Si(100) substrates are very few, and moreover they are limited in crystallographic investigations [7,8]. The most significant problem of the (100) oriented GaAs-on-fluoride was antiphase disorder which generates in GaAs layers. However at present, its generation mechanism is being clear and the suppression method is being developed [5,6,7].

In this work, the first device fabrication on the GaAs/fluoride/Si structure was demonstrated, where double-layered $(Ca,Sr)F_2/CaF_2$ was introduced as the fluoride layer and off-oriented Si(100) and Si(511) substrates were used.

2. Variation of GaAs/Fluoride/Si Structures

Various composition of the fluoride layer between GaAs and Si can be considered as shown in Fig.1. The GaAs/CaF_2/Si structure shown in Fig.1(a) is most simple and the crystallinity of the GaAs layer was best as long as it was measured by Rutherford backscattering and channeling spectroscopy[8]. However, it has a problem of the lattice mismatch between GaAs and CaF_2. If CaF_2 is replaced by $(Ca,Sr)F_2$, the lattice matching condition between fluoride and GaAs is satisfied. However, direct growth of single crystalline $(Ca,Sr)F_2$ films on Si(100) face is difficult [9]. So, a double-layer structure composed of $(Ca,Sr)F_2/CaF_2$ shown in Fig.1(b) is a good candidate for solving the conflicting problem.

In growth of GaAs on the fluoride crystal of (100) face, there is a problem of antiphase disorder, which results from four-fold symmetry of atomic arrangement of the (100) face of CaF_2 structure and/or the micro facets existing on the as grown fluoride films [5]. In order to suppress the antiphase disorder, use of off-oriented substrates and planarization of the micro facets by rapid thermal annealing (RTA) were found to be effective [6,10]. Recently, single domain GaAs with good surface morphology was obtained in the structure as shown in Fig.1(c), where a Si(511) substrate was used and the surface of CaF_2 was planarized by the RTA process [7]. The double-layer structure shown in Fig.1(b) is also considered to be useful from a viewpoint of the suppression of antiphase disorder, since the micro facets on the $(Ca,Sr)F_2$ surface are intrinsically deformed or truncated compared with those on CaF_2 surface [6]. Thus, the epitaxial growth of GaAs films on the mixed fluoride is also tried.

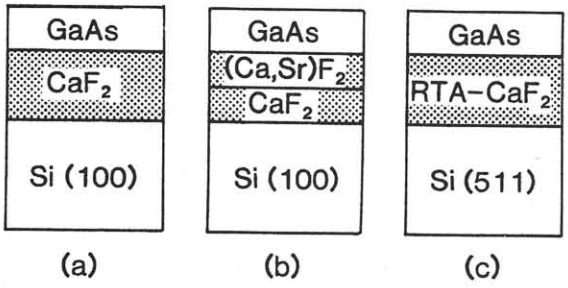

Fig.1 GaAs/fluoride/Si structures grown for FET fabrication in this work.

3. Growth of GaAs/Fluoride/Si Structures

Si(100) just and 4° off toward [011] wafers were chemically cleaned and heated in a UHV chamber at 830°C for 30min. On these in-situ cleaned substrates, 200nm-thick CaF_2 layers were epitaxially grown at 550°C and 100nm-thick $Ca_xSr_{1-x}F_2$(x=0.5) layers were grown at 500°C on the CaF_2 layers continuously. In some samples, only CaF_2 layers were grown for comparison. Besides (100) samples, 300nm-thick CaF_2 layers were grown on Si(511) substrates in the same way as on Si(100) substrates, and in-situ RTA at 900°C for 90sec was carried out [7]. After growth of the fluoride layers on the Si substrates, GaAs layers were grown on these samples by MBE. In the growth of GaAs, the

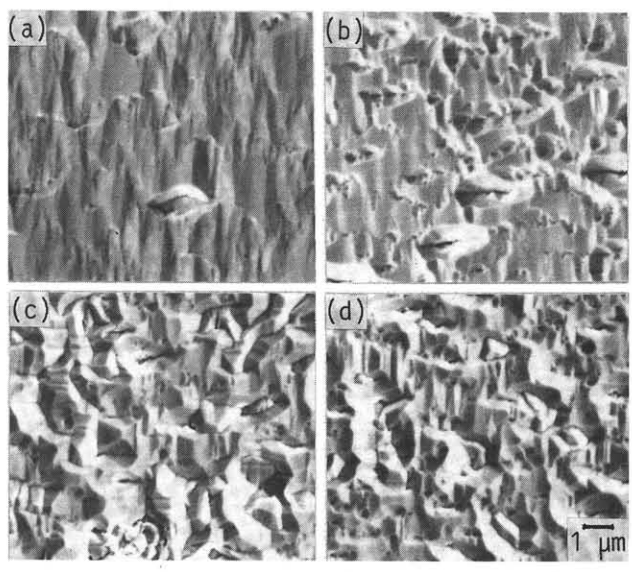

Fig.2 Surface morphologies of GaAs grown on fluoride/Si(100) structures. The fluoride layer and off-set angle of Si substrates are: (a) $(Ca,Sr)F_2/CaF_2$, 4°off (b) CaF_2, 4°off (c) $(Ca,Sr)F_2/CaF_2$, just, (d) CaF_2, just

2-step growth method (450°C-580°C) was employed, in which 1.3μm-thick un-doped buffer and 0.2μm-thick Si-doped ($2x10^{17}cm^{-3}$) active layers were grown.

Fig.2 shows surface morphologies of these samples. A GaAs layer grown on the $(Ca,Sr)F_2/CaF_2$/off-oriented Si(100) structure showed a smooth surface and almost single-domain structure though a few antiphase regions were found as shown in the photograph (Fig.2(a)). When GaAs layers were grown directly on CaF_2 layer, density of antiphase regions drastically increased, even though Si substrates were off-oriented (Fig.2(b)). The surface of the GaAs/fluoride structure grown on just(100) substrates showed random antiphase structures for both fluoride layers of CaF_2 and $(Ca,Sr)F_2/CaF_2$ (Fig.2(c)(d)).

4. MESFET Fabrication and Characteristics

MESFET's were fabricated in a conventional process on the GaAs-on-insulator structure as shown in Fig.3. First, each device was isolated by mesa-etching the Si-doped active layer in $4H_2SO_4:H_2O_2:H_2O$ solution. After the mesa-etching, sources and drains were formed by Au/Au-Ge using the lift-off technique and sintering at 450°C for 90sec in N_2 atmosphere. Finally, the Au gate electrodes were formed, also by the lift-off technique.

Fig.4 shows a micrograph of a fabricated FET, where the gate length(Lg) and the gate width(Wg) are 3μm and 60μm, respectively. Fig.5 shows an example of the drain current (I_d) and drain voltage (V_d) characteristics of an FET fabricated on a GaAs/$(Ca,Sr)F_2/CaF_2$/Si(off-(100)), where Lg=7μm and Wg=140μm. Normal FET operation was obtained and the maximum value of gm was 12mS/mm at V_g=+0.7v. The FET's fabricated on other specimens also showed the normal operation. Fig.6 shows $\sqrt{I_d}$ -V_g

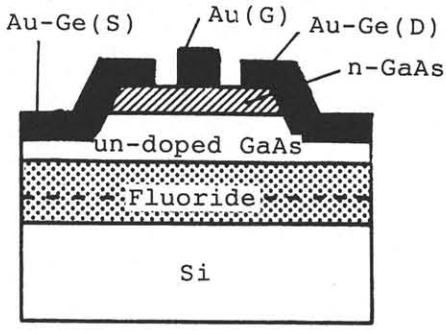

Fig.3 Schematic of a MESFET fabricated on a GaAs/fluoride/Si structure. The fluoride layer is $(Ca,Sr)F_2/CaF_2$ or CaF_2.

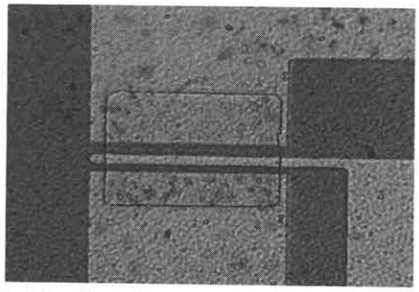

Fig.4 Optical micrograph of plan view of a fabricated MESFET of which cros-sectional structures is shown in Fig.3. Lg/Wg=3μm/60μm.

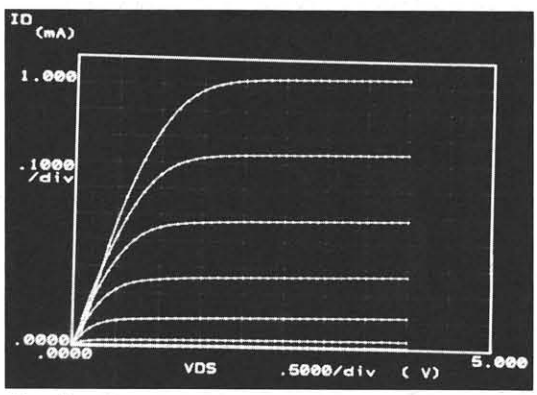

Fig.5 I_d-V_d characteristics of a fabricated FET. Vg=+0.8V -0.4V with 0.2V step. Lg/Wg=7μm/140μm. gm=12mS/mm at Vg=+0.7V and $K=0.80mA/V^2$.

characteristics at the saturation regions of these FET's. Characteristics of an FET fabricated on a homoepitaxial substrate ($1.0x10^{17}cm^{-3}$ Si-doped in active layer) are also shown as a reference. The K-values and V_{th} are summarized in Table 1. The highest K-value of $0.8mA/V^2$ was obtained on GaAs/$(Ca,Sr)F_2/CaF_2$/Si using off-oriented

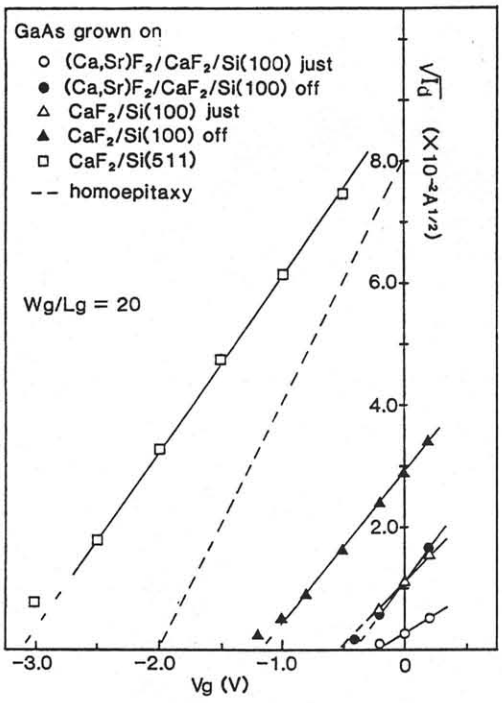

Fig.6 $\sqrt{I_d}$- V_g characteristics of FET's fabricated on each structure and those on GaAs-homoepitaxial layer for comparison.

Substrate	Si(100)				Si(511)	GaAs(100)
Fluoride	$(Ca,Sr)F_2/CaF_2$		CaF_2		CaF_2(RTA)	homoepi.
off/just	off	just	off	just		
$K(mA/V^2)$	0.8	0.2	0.6	0.5	0.6	1.6
V_{th} (V)	-0.5	0.0	-1.2	-0.5	-3.2	-2.0
$N_D(cm^{-3})$	<---------		$2x10^{17}$		---------->	$1x10^{17}$

Table 1 K, V_{th}, N_D(amount of doped Si) of FET's fabricated on each structure.

(100) substrates, whose surface morphology was very good as shown in Fig.2(a). This value is as high as the best value obtained on GaAs/$(Ca,Sr)F_2$/GaAs structure [4].

In all FET's fabricated on GaAs-on-fluoride, the V_{th} values were higher than the calculated value assuming that all doped Si atoms were activated as donors (that is -5V for $N_D=2x10^{17}cm^{-3}$). This decrease of the carrier density is supposed to be caused by crystalline defects in GaAs layers, and the lower V_{th} on the (511) substrate than those on (100) substrates is probably related to the lower dislocation density in the GaAs layer grown on (511) substrate, as observed by cross-sectional TEM [7].

5. Conclusion

MESFET's were fabricated on GaAs/fluoride/Si structures and $K=0.8mA/V^2$ with Lg/Wg=7μm/140μm was obtained on a single domain GaAs layer. This single domain layer was grown by using the double-fluoride layer composed of $(Ca,Sr)F_2/CaF_2$ and on off-oriented (4° toward [011]) Si(100) substrate. These results demonstrate feasibilities of GaAs/fluoride/Si structure for device applications.

Acknowledgments

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