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An Electron Counting Detector for CCD Image Sensors

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A new electron counting detector, named a "double gate floating detector", has been proposed and fabricated. At room temperature, it achieves an equivalent number of noise electrons of 0.5 electron rms and a dynamic range of 79dB over a 3.58MHz video bandwidth. For the first time in the world, an equivalent number of noise electrons under one electron rms has been realized for a CCD detector in a wide video bandwidth. The dynamic range has been improved by a factor of 6, compared to that for a conventional "floating well detector".

1.INTRODUCTION

A buried channel charge coupled device (CCD) has realized complete signal charge transfer. Therefore, it introduces no transfer noise. However, conventional charge detectors, incorporated into CCDs, have comparatively large noise, which consists of thermal noise and 1/f noise from MOS transistors. In order to exploit CCD performances effectively, a high sensitivity, low noise and wide dynamic range charge detector is required. The authors proposed a high sensitivity detector, a "floating well detector" at IEDM 1987 (1). However it has handled a small amount of signal charges of 2000 electrons. So, its dynamic range is not sufficient for CCD imagers. This paper describes a low noise and wide dynamic range detector, named a "double gate floating surface detector". This detector yields an equivalent noise of 0.5 electron, so that it can be used as an electron counting detector. The 79dB dynamic range is sufficent for a CCD image sensor detector.

2.DEVICE STRUCTURE

The "double gate floating surface detector" principle is a combination of an n-type buried sensing channel and a p-channel surface detection transistor across it(2)(3). Figure 1 shows a cross-sectional view of the detection transistor across the sensing channel. A shallow p-well with a sensing channel in it and source/drain p+ regions are formed on an n-type substrate. The shallow p-well under a sensig channel is completely depleted. Charge packets, clocked along the CCD channel, are transfered into the sensing channel. The p-type channel for the detection transistor lies at the silicon-silicon dioxide interface. The charge packets modulate channel conductance in the detection transistor.

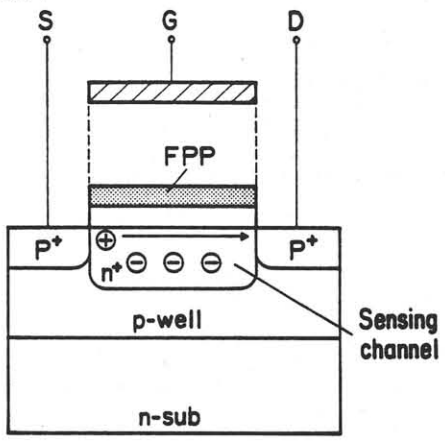


Fig.1 Detection transistor cross-section.

The sensing capacitance for the detection transistor can be smaller than that for the widely used "floating diffusion detector". The small sensing capacitance has been achieved by the smaller sensing region, in which the sensing channel and the p-type channel for the detection transistor are crossed. Moreover, a "double gate structure" is introduced for smaller sensing capacitance. In this structure, the 10000Å thick oxide is applied to a detection transistor gate oxide. An FPP (flat potential plate), which is floating electrically, is inserted under the detection transistor gate(G). The FPP suppresses the two dimensional effect, which causes a potential pocket in the sensing channel(1). The transfer loss, induced by a potential pocket, results in transfer noise in the detector.

Figures 2(a) and (b) show a detector plane structure and a cross-section at A-A′, respectively. The signal charge(electron) packets are clocked along the three phase CCD($\phi_1 \sim \phi_3$) channel, and transferred into the sensing channel underneath the p-type channel for the detection transistor. The detected signal charge packets are moved out into a reset drain(RD) by applying a positive pulse on a reset gate(RS).

Dimensions are a 4×4μm gate area with a 10000Å thick gate oxide and a 1200Å thin gate oxide under the FPP. In order to form the n-type sensing channel under the detection transistor gate region, an additional local phosphor implantation is needed. The source(S) and drain(D) regions for the p-channel detection transistor are made in self-alignment with the output gate(OG), the reset gate(RS) and the FPP. The source region is connected to the p-channel load transistor, which is made by a junction FET, and to the source follower, which consists of n-type channel MOS transistors.

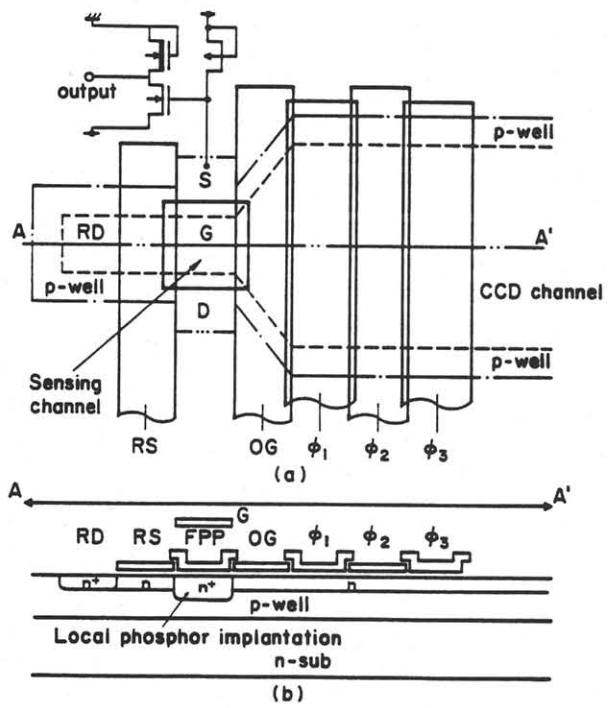


Fig.2 Practical output amplifier fabricated in shallow p-well on n-type substrate.
(a) Structure of the detector
(b) Cross-section at A-A′ in Fig.2(a)

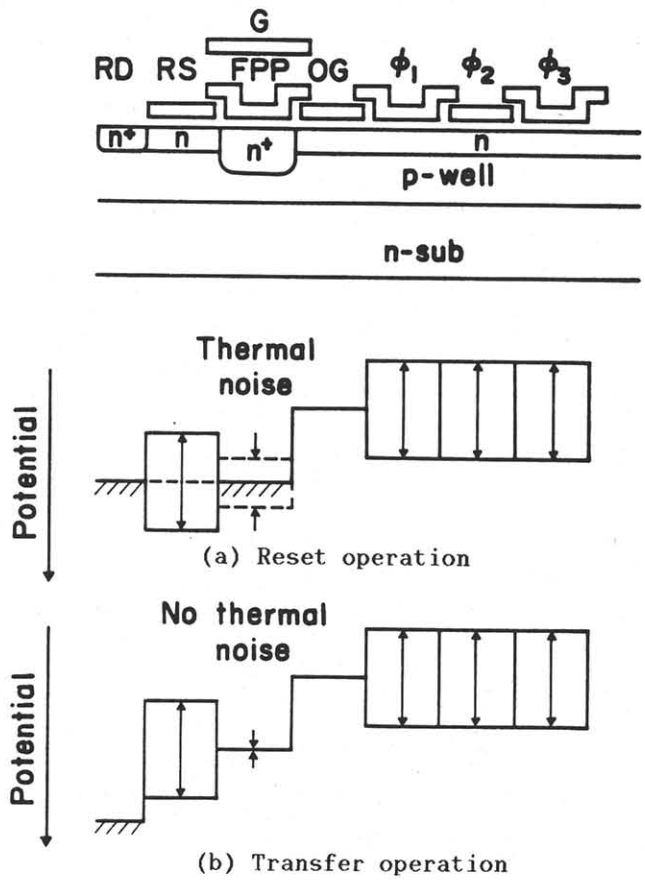
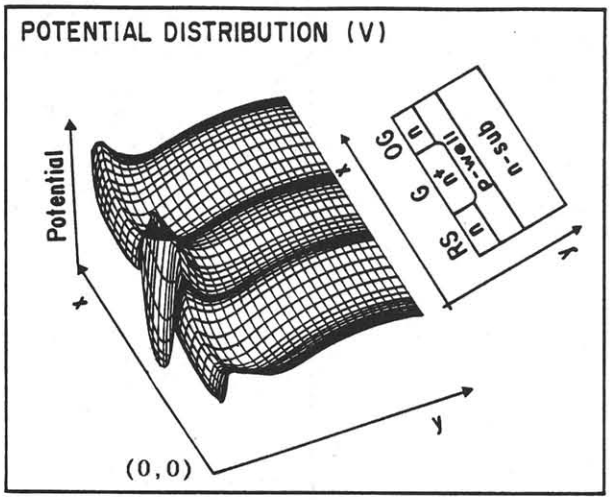
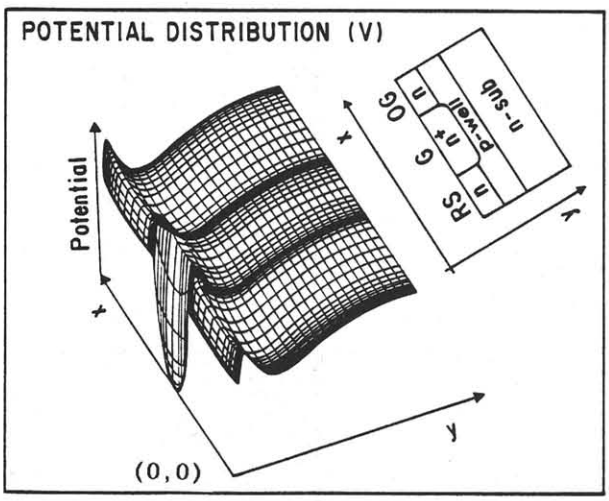


Fig.3 Channel potential diagram.

Figures 3(a) and (b) show the potential diagrams in reset operation and in transfer operation, respectively(1). In the reset operation, residual charge in the sensing channel includes noise charge, which is caused by thermal noise (KTC noise) from reset gate resistance. On the other hand, in the transfer operation, no charge exists in the sensing channel, because signal charge is completely transferred out into the reset drain(RD).



(a) No signal charge



(b) 3600 electrons signal charge

Fig.4 Potential distribution in Fig.2(b) structure.

3.DEVICE SIMULATION

The authors examined a "double gate floating surface detector" performance with a two dimensional device simulator, before fabricating it. The simulated structure is shown in Fig.2(b). Figures 4(a) and (b) show the potential distributions for no signal charge and for 3600 electrons signal charge, respectively. The potential level at Y=0 in Fig.4 indicates the surface potential. The first maximun potential level along the Y axis, indicates the buried channel potential. As shown in Fig.4(b), the surface potential in the detector section is made lower by signal charge, compared to that for no signal charge. The amount of signal charge and the difference in the surface potentials, between Figs.4(a) and (b), give sensing capacitance, which corresponds to responsivity for the detector. The results are shown in Fig.5. The dot-dashed line in Fig.5 shows the simulated responsivity. For detection transistor gate oxide thickness 10000Å the respectively is 150 μv/electron.

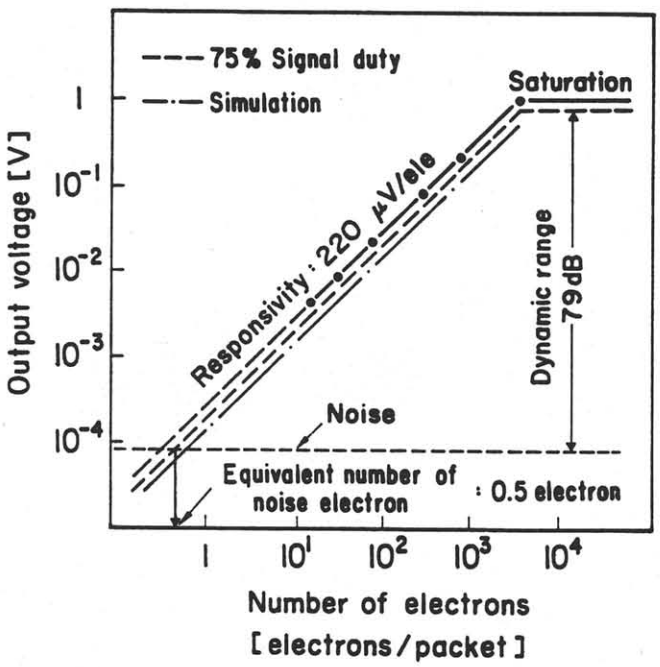


Fig.5 Responsivity and output noise.

4.EVALUATION

The device was evaluated at a 7.16MHz clock frequency, that is twice the NTSC color subcarrier frequency. The signal duty defined by the signal output period in the clock cycle was approximately 75%, which was determined by a 35nsec positive reset pulse.

The measured responsivity of this detector is shown in Fig.5 as a solid line. It was measured by injecting a series of charge packets into the sensing channel. The responsivity is liner over a charge packets range from 20 to 4500 electron/packet, and it is as high as 220 μv/electron. The measured responsivity is lower than the simulated value by about 30%. A three dimensional device simulation may be needed for more accurate estimation, because the difference between the measurement and the calculation may be due to potential distribution perpendicular to the signal electron transfer direction.

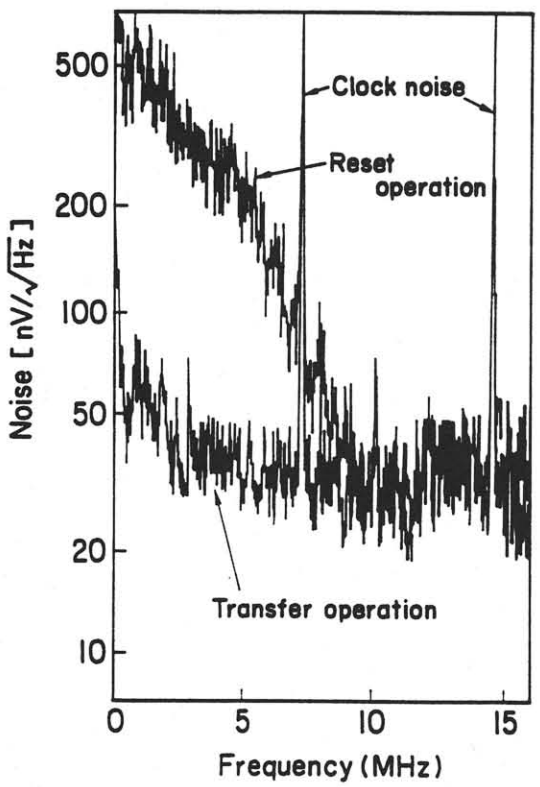


Fig.6 Noise spectra for output amplifier in reset operation and in transfer operation.

The output noise for the new detector was measured by the spectrum analyzer. Figure 6 shows noise spectra for the device, both in the case of reset operation and in the case of transfer operation. In the reset operation there is a reset noise(KTC noise) which is caused by the thermal noise in the reset gate(RS). In the transfer operation, the reset noise is completely suppressed. The overall RMS noise value, within the band 10KHz-3.58MHz, is 84μv rms, in the transfer operation at room temperature.

The noise level is 84μv rms and a signal duty ratio is 75%. Thus the equivalent number of noise electron is as low as 0.5 electron. A saturation level is 4500 electrons and the noise level is 0.5electron, so the dynamic range is as wide as 79dB.

5.CONCLUSION

A new high sensitivity charge detector has been fabricated. It yields the 0.5 electron rms equivalent number of noise electrons and a dynamic range of 79dB. For the first time in the world, an equivalent number of noise electrons, under one electron rms, has been realized over a 3.58MHz video bandwidth. The "double gate floating surface detector" has sufficient performance for its successful use as a CCD image sensors detector.

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