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Analysis of Charge Transfer Loss in Dual Read-Out Registers Used for HDTV CCD Image Sensor

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Dual read-out register structure is indispensable for high definition television (HDTV) CCD image sensors to realize high signal read-out frequency (74.25MHz). However, this structure would suffer from a charge transfer loss between two read-out registers, unless precise care was taken in designing the registers. This paper describes the charge transfer loss mechanism and proposes a new dual register structure, which can eliminate this problem. As a result, the charge transfer loss is completely suppressed.

1. INTRODUCTION

Recently, a high definition television (HDTV) CCD image sensor, overlaid with an amorphous silicon photoconversion layer, has been reported[1]. The HDTV image sensor has advantages of high sensitivity and wide dynamic range. The image sensor realizes high speed signal read-out frequency (74.25MHz), by using a dual horizontal CCD (H-CCD) register structure.

However, unless precise care is taken in designing the dual H-CCD registers, a charge transfer loss will occur between two H-CCD registers[2]. Also, the transfer loss becomes larger as H-CCD register width becomes wider, because the time required for the charge transfer becomes longer. Therefore, it is a serious problem for the image sensor because of the wide channel width (24μm) H-CCD register that maintains high signal charge handling capability, resulting in a wide dynamic range.

This paper describes the transfer loss mechanism and proposes a new dual H-CCD register structure. Due to the new structure, a high signal charge handling capability (2×10^5 electrons/pixel) HDTV CCD image sensor without the charge transfer loss has been realized.

2. CHARGE TRANSFER LOSS IN DUAL REGISTERS

The charge transfer loss causes signal charge interfusion between two H-CCD registers and generates fixed pattern noise (FPN) on a reproduced image, as follows.

Figure 1(a) illustrates the charge transfer from vertical CCD (V-CCD) registers into two H-CCD registers. Figure 1(b) shows clock pulse waveforms, applied to each electrode during the transfer period. The odd numbered row signal charge,Qo, is transferred into the 1st H-CCD register, while the even numbered row signal charge,Qe, is transferred into the 2nd H-CCD register through transfer gate (① and ②). Qo and Qe are transferred in the horizontal direction and read out in output terminals(③).

However, when Qe is transferred from the 1st H-CCD into the 2nd H-CCD, transfer loss occurs and a part of Qe (Qr) remains in the 1st H-CCD. Therefore, the signal charges read out from the 1st H-CCD and the

2nd H-CCD become Qo+Qr and Qe-Qr, respectively. Thus, the signal charge interfusion between two H-CCD registers occurs. As a result, the FPN appears on a reproduced image.

Figure 2 shows the FPN in the device with conventional dual H-CCD registers shown in Fig.1. The FPN has a white-and-black vertical line pair pattern and degrades image quality.

3. MECHANISM

It is known that a thermal diffusion transfer mode, which is one of the charge transfer modes in CCD, has the slowest charge transfer speed. The transfer time constant for the mode, which is estimated from a theoretical formula, is 0.1μsec for the dual H-CCD registers described above. However, a transfer time constant, which was measured experimentally, was about 0.5μsec. Therefore, the cause of charge transfer loss between the two H-CCD registers cannot be explained with the thermal diffusion transfer mode.

The authors have further examined the cause of the transfer loss. As a result, it has been clarified that the transfer loss is caused by channel potential fluctuation, which is formed by H-CCD transfer electrode edge ruggedness, as follows.

Figure 3 is an SEM photograph of the H-CCD polysilicon transfer electrodes. It is observed that the electrode edges are rugged. The magnitude of ruggedness,R, is about 0.2μm.

Figure 4(a) shows the 1st H-CCD register, in which the electrode edge ruggedness is modeled. The channel, where charge Qe is transferred, is between both side 2nd polysilicon transfer electrodes. Transfer channel width x is 4.1μm on an average and fluctuates continuously along the Y-Y' direction, due to the 2nd polysilicon ruggedness. Therefore, channel potential fluctuation occurs, because of narrow channel effect.

Figure 4(b) shows the channel potential profile and transfer loss for Qe. A part of Qe (Qr) remains in potential pockets, which are formed by the channel potential fluctuation. Therefore, transfer loss occurs between two H-CCD registers. The potential depth and potential gradient in the pockets are about 30mV and 30mV/μm, respectively. Their values were estimated by arbitrary shape simulation[3].

4. NEW DUAL READ-OUT REGISTERS

As seen from the mechanism described in the previous section, it is expected that the transfer loss would be suppressed if the potential pockets were practically removed, by forming a more than 30mV/μm electric field along the transfer direction.

Figure 5 shows a new dual H-CCD register structure. Two barrier potential areas are formed in the 1st H-CCD register by double boron ion implantations, in order to form the electric field and remove the potential pockets.

Figure 6 shows the channel potential profile in the new dual H-CCD registers, which is estimated by simulation. Due to forming the barrier potential areas, the weakest fringe electric field in the charge transfer direction becomes 30mV/μm, in the case of no potential pocket. Therefore, the potential pockets will be removed and charge transfer loss will not occur.

Figure 7 shows measurement results of the charge transfer loss in the new dual H-CCD registers and the conventional dual H-CCD registers. In the charge transfer from the 1st H-CCD register into the 2nd H-CCD register, residual charge,Qr, becomes below the measurement limit in the new dual H-CCD registers, while Qr is 1.0×10^{2}

electrons/pixel at even the longest transfer period (T=1.7μsec) in conventional dual H-CCD registers. Thus, this result proves that the new dual register structure enables signal charge Qe to be completely transferred between the two H-CCD registers.

Figure 8 shows a reproduced image in the HDTV CCD image device with new dual H-CCD registers. In this device, there is no interfusion between odd and even numbered row signal charges and no FPN occurs.

5. CONCLUSION

In a dual read-out register CCD image sensor,the transfer loss mechanism has been clarified. The transfer loss is caused by potential fluctuation, which is formed by the transfer electrode edge ruggedness. A new structure for the dual H-CCD registers, which have two barrier potential areas to remove the potential pockets practically, has been proposed. As a result, an HDTV CCD imager, which has no charge transfer loss between the two H-CCD registers and high signal charge handling capability (2×10^5 electrons/pixel), has been realized.

6. REFERENCES

1) S.Manabe et al.; ISSCC Dig. Tech. Papers, (1988) pp50-51.
2) K.Orihara and E.Oda; IEDM Tech. Dig., (1986) pp365-368.
3) S.Osawa et al.; Jpn. Soc. Appl. Phys., (1987) 18a-ZK-2.

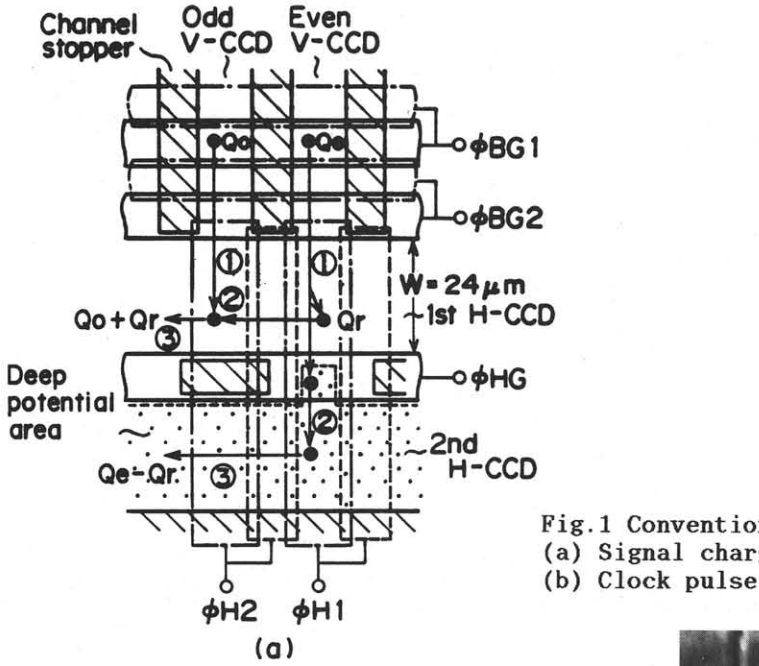

Fig.1 Conventional dual H-CCD read-out registers.
(a) Signal charge transfer from V-CCD into H-CCD.
(b) Clock pulse waveforms during the transfer period.

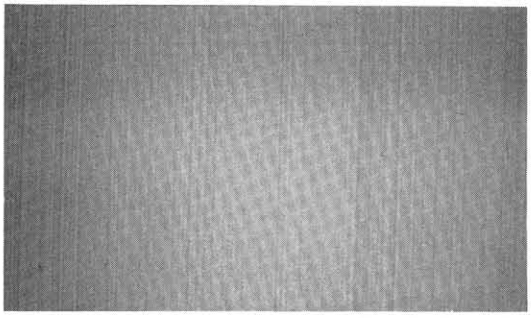

Fig.2 White-and-black vertical line pair FPN on a reproduced image.

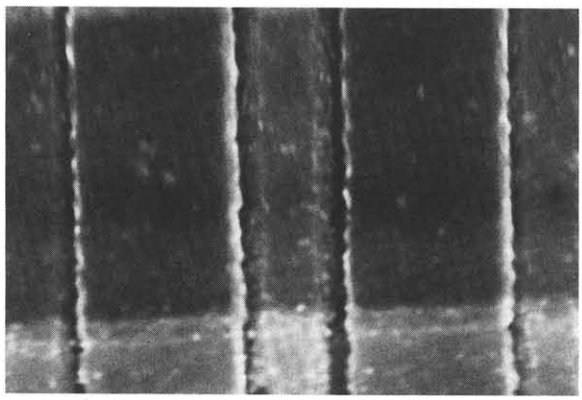

Fig.3 SEM photograph of H-CCD polysilicon transfer electrodes. Ruggedness is observed at the transfer electrode edges.

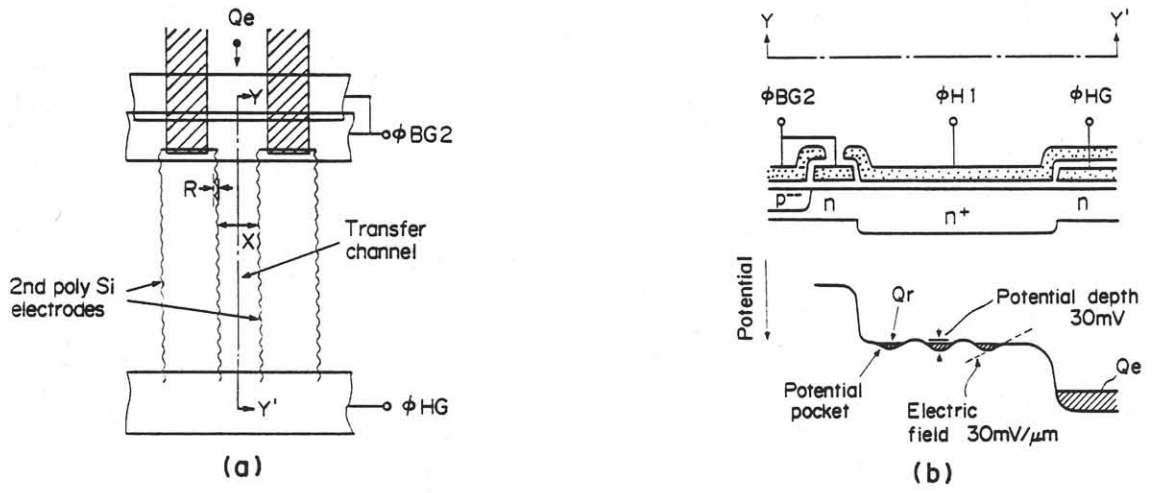

Fig.4 1st H-CCD register region detail drawing for illustrating charge transfer loss mechanism.
(a) Electrode edge ruggedness is emphasized. Transfer channel width x is defined by the space between 2nd polysilicon electrodes.
(b) Charge transfer loss occurs due to potential pockets.

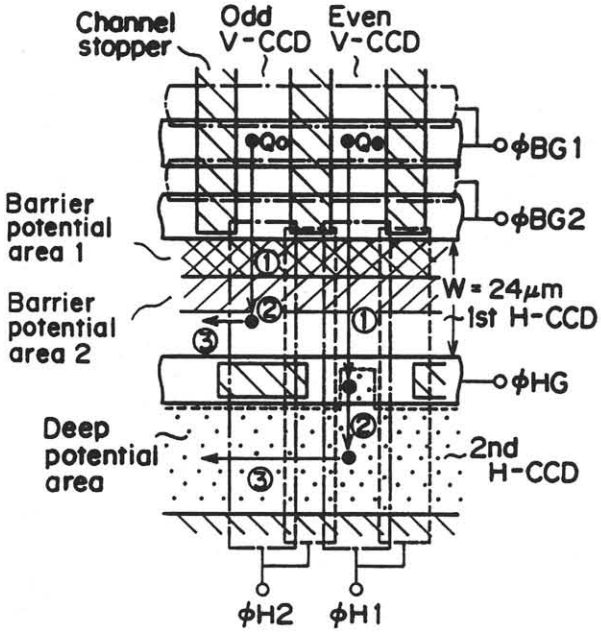

Fig.5 New dual H-CCD register structure. Two barrier potential areas are formed in the 1st H-CCD register.

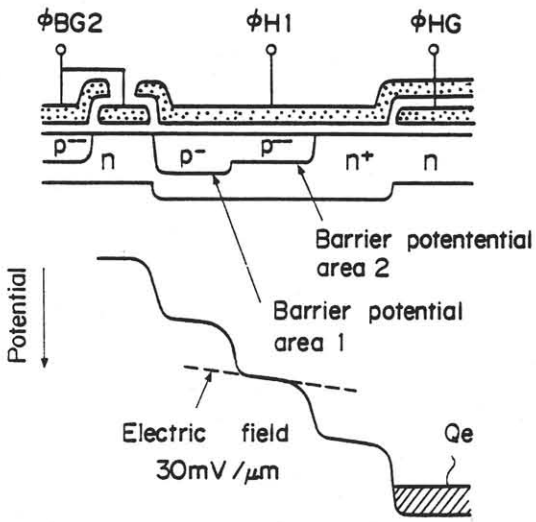

Fig.6 Channel potential profile in the new dual H-CCD registers.

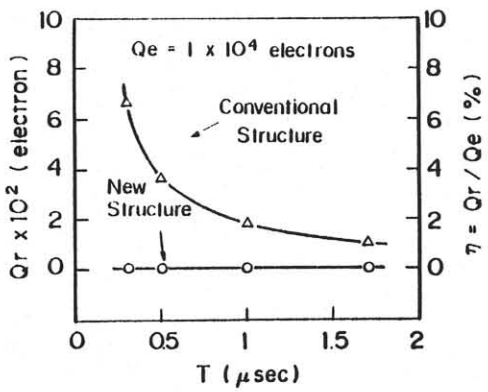

Fig.7 Measurement results of charge transfer loss in new dual H-CCD registers and conventional dual H-CCD registers.

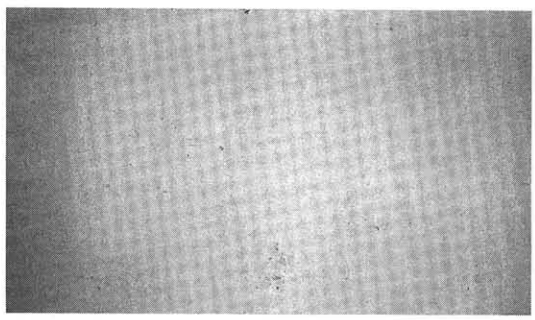

Fig.8 Image reproduced by an HDTV CCD image sensor with new dual H-CCD registers.