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GaInAsP on Si Substrates and Its Device Application

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The performance of photonic and electronic devices fabricated with InP and related compounds on silicon substrate has advanced to the degree that this technology may be considered for device applications. In this talk, the recent advances on the growth, characterization, and applications of GaInAsP-InP lattice matched system on Si substrates using low pressure metalorganic chemical vapor deposition growth, are presented.

INTRODUCTION

Long distance optical links use semiconductor lasers emitting at 1.3 μm and 1.55 μm fabricated by materials such as GaInAsP-InP lattice matched system on InP substrate. Unfortunately the technology of integrated circuits for signal treatment is more difficult on this material than on GaAs substrates. Since the technology of silicon is more advanced than GaAs, and InP based materials, the solution is to combine the advantages of InP and GaAs devices with the maturity of Si processing technology, using existing Si integrated circuit equipment.

However, device quality of InP, or GaAs based materials has not been obtained by direct growth on Si substrates, since the lattice parameter, crystal symmetry, thermal expansion coefficient of InP, GaAs and Si are different. Furthermore, nucleation of InP and GaAs on Si substrate is difficult.

At the present stage of III-V/Si technology development, attention is focused on perfecting the growth of InP, GaAs and related compounds on Si and demonstrating that devices with acceptable operating characteristics can be fabricated in these layers.

The most important problems that are encountered, when growing III-V semiconductors on Si substrates are as follows:

1) The difference of lattice parameter between III-V semiconductor and Si substrate.
2) The difference of lattice symmetry.
3) The difference of thermal expansion coefficient.

1) The difference of lattice parameter

8% lattice mismatch between InP and Si, and 4% between GaAs and Si, produces misfit dislocation at the interface. The formation of misfit dislocations and the introduction of tensile stress in the heteroepitaxial InP, GaAs based materials on Si are the principal problems for the application of these materials for minority carrier devices such as laser. The dislocations at the III-V/Si interface do not degrade the III-V epilayer crystalline quality. Instead, it is the propagation of dislocations away from the interface region (the so-called threading dislocation) that appears to be primarily responsible for the nonradiative recombina-

tion centers, the threading dislocations also reduce minority carrier lifetimes, presenting inferior properties of devices fabricated on III-V epilayers on Si substrates.

Therefore very low misfit dislocation densities in the III-V epitaxial overlayers are essential for laser application.

In order to reduce the misfit dislocations in GaInAsP-InP layers grown on Si substrate, using low pressure metalorganic chemical vapor deposition, we used at first two step growth, i.e. first a thin layer of 200 Å of GaAs is grown at 450°C, using a growth rate of 50 Å/min. Then the substrate temperature is raised to 550°C. A 5 periods lattice matched superlattices of GaInAsP-InP or GaAs-GaInP with Lz = 100 Å and L_B = 100 Å (L_B is the thickness of InP or GaInP barrier, and Lz is the thickness of GaInAsP or GaAs quantum well), have been grown. These superlattices have been shown effective in bending dislocation lines out toward the edges of the crystal, preventing the cross doping of the epilayer with Si, and preventing dislocation movement in device operation.

2) The difference of lattice symmetry

One of the problems in growing GaInAsP-InP (polar semiconductor) on Si (non polar semiconductor) is the possible occurrence of antiphase domains. In certain regions of the epilayer the cation and anion sublattices have been interchanged. The interface between domains with opposite sublattice allocation forms a two-dimensional structural defect called an antiphase boundary[1]. Antiphase boundaries in InP contain In-In and P-P bonds represent an electrically charged defect. The In-In bonds act as acceptors; the P-P bonds as donors. In general, antiphase boundaries which act as highly compensated doping sheets with very little net doping can also act as nonradiative recombination centers.

In order to eliminate the antiphase domain, in GaInAsP-InP layers grown on Si by LP-MOCVD, we used a 4° off (100) towards (011) oriented Si substrates, and we performed the high temperature annealing (1000°C) under AsH_3-PH_2 of titled substrate prior to growth, in order to form the double atomic layer steps, which help eliminate antiphase domains[1].

3) The difference of thermal expansion coefficient

The difference in thermal expansion coefficients of InP and related compounds with Si substrates puts the epilayer under extreme tensile stress. The difference in the lattice parameters parallel and perpendicular to the interface arises from the difference in thermal expansion between InP and Si, not from misfit accommodation by elastic strain.

Analyses of the tetragonal distortion in InP on Si would thus be expected to yield information concerning the defect structure in this material.

GaInAsP-InP on Si and ITS DEVICE APPLICATION

Because of application of long wavelength components, especially 1.3 μm and 1.5 μm lasers, quaternary compounds $Ga_xIn_{1-x}As_yP_{1-y}$ ($0 \leq X \leq 0.47$ and $0 \leq Y \leq 1$) lattice matched to InP have become very important materials for the optoelectronic industry, and it would be of great interest to combine these materials with Si technology.

The lattice parameter of quaternary compound of composition $Ga_xIn_{1-x}As_yP_{1-y}$ is given by[2]:

$$a(x,y) = a(GaAs)\,XY + a(InAs)(1-X)Y + a(GaP)X(1-Y) + a(InP)(1-X)(1-Y)$$

The coefficient of linear thermal expansion $\alpha(XY)$ of the quaternary compound may also be calculated using Vegard's law:

$$\alpha(X,Y) = [\alpha(GaAs)a(GaAs)XY + \alpha(InAs)a(InAs)(1-x)Y + \alpha(GaP)a(GaP)X(1-Y) + \alpha(InP)a(InP)(1-x)(1-Y)]/a(X,Y)$$

The thermal expansion coefficient of GaP is 5.3×10^{-6} (K^{-1}), InAs is 0.011×10^{-8} (K^{-1}), InP is 4.56×10^{-6} (K^{-1}), GaAs is 5.7×10^{-6} (K^{-1}) and Si is 2.6×10^{-6} (K^{-1}). The difference between the mean linear coefficients of thermal expansion of InP and Si is less than 1/4 the difference between those of GaAs and Si. In addition, deposition temperature of the LP-MOCVD growth of GaInAsP-InP are typically 550°C whereas MOCVD GaAlAs-GaAs films are grown at 750°C. As a result of the lower thermal expansions and the lower growth temperature, the thermally-induced stress in GaInAsP-InP/Si films due to cooling from the growth temperature is less than for GaAs-GaAlAs/Si layers of comparable thickness.

Our preliminary results of GaInAsP-InP/Si lasers[3-7] show that the solution the problem of degradation of GaAlAs-GaAs/Si lasers is to substitute GaInAsP-InP/Si lasers instead. It is known that InP-based long wavelength lasers are more "immune" to the deleterious effects of stress than are GaAs-based lasers[8-9]. As a result, the lifetimes of heteroepitaxial GaInAsP-InP lasers grown on Si substrate may be longer than those of GaAlAs-GaAs/Si lasers although the lattice mismatch of InP/Si is 8% compared to 4% for GaAs/Si.

The growth of GaInAsP-InP double heterostructure grown by LP-MOCVD is reported for the first time by Razeghi et al.[3] using LP-MOCVD. X-ray diffraction patterns, as well as structural characterizations, indicate that the layers have very good crystalline quality. An intense photoluminescence signal from the quaternary alloy $Ga_xIn_{1-x}As_yP$ has been recorded at room-temperature, at the exptected value of 1.3 μm[6].

LIGHT EMITTING DIODES of GaInAsP-InP on Si

We fabricated for the first time an InP-GaInAsP light emitting diode, emitting at 1.15 μm grown by LP-MOCVD on Si substrate. The epitaxial structure has been grown by LP-MOCVD on (100) Si (n^+) substrate misoriented 4° towards (110). The structure of the devices include: i) 10 periods GaAs-GaInP superlattice undoped as buffer layer, with Lz(GaAs) = 50 Å and $L_B(Ga_{0.49}In_{0.51}P)$ = 50 Å thick. ii) 2 μm InP sulphur doped as n-type confinement layer. iii) 2000 Å GaInAsP (λ = 1.15 μm) undoped active layer. iv) 500 Å InP zinc doped as P-type confinement layer. Then the stripes of 1 μm width by using photolithography followed by chemical etching. The stripe to stripe spacing is about 300 μm. In a second growth step, we covered the stripes with 1 μm InP, Zn doped as a P-type confinement layer and 0.5 μm thick $Ga_{0.47}In_{0.53}As$: Zn doped as P-type contact layer. We have put these diodes under continuous wave operation for 24 hours, with an injection current of 200 mA. We did not observe any degradation. The devices may be useful for optical interconnexion between Si chips already processed as electronic IC's[4].

1.3 μm GaInAsP-InP LASER on Si

We fabricated the first successful room-temperature GaInAsP-InP double heterostructure laser emitting at 1.27 μm grown by LP-MOCVD. The layers grown for these devices were as follows:

i) 500 Å undoped GaAs as accommodated layer.

ii) 5 periods GaInAsP-InP superlattice with

L_B = 100 Å and Lz = 100 Å, for elimination of mismatch dislocations.

iii) 3-μm InP (S) doped with $N_D-N_A \simeq 10^{18}cm^{-3}$ as n type confinement layer.

iv) 0.2 μm $Ga_{0.25}In_{0.75}As_{0.5}P_{0.5}$ undoped active layer.

v) 1 μm InP(Zn) doped as a P type confinement layer.

vi) 0.5 μm $Ga_{0.47}In_{0.53}As$, Zn doped ($N_A-N_D \simeq 10^{19}$ cm^{-3}) as a cap layer.

Gain-guided oxide-defined stripe-geometry lasers were fabricated. The devices were cleaved, producing the diodes with 200 μm cavity length and 12 μm strip width. The threshold current density of 10 KA/cm^2, with an external quantum efficiency of 10% per facet and an output power of 20 mW have been measured. Preliminary aging test have been processed in pulse conditions at room-temperature. After an equivalent CW aging time of 80 seconds, under driving pulses of 50 ns at 5 KHz, an increase of threshold current $\Delta I_{th}/I_{th}$=7% is measured with an output power of 3 mW, without any degradation of differential quantum efficiency. These results are very promising compared to recently published aging test of GaAs lasers on Si[10]. The CW measurements are under study and the results will be presented.

These results are very promising for future monolithic integration of optoelectronic devices on Si substrate.

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