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Stress-Released MBE Growth of GaAs on Si (001) with a Si-GaAs Superlattice Buffer

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GaAs hetero-epitaxial layers grown on Si substrates were investigated by RHEED, X-ray diffrction and stress gauge measurements. Si-GaAs superlattice buffer layers were introduced to reduce the stress in thick GaAs films grown on Si substrates. Tensile stresses due to a thermal expansion coefficient mismatch balanced with compressive stresses due to a lattice constant mismatch at a substrate temperature of about 500 °C.

1. Introduction

The epitaxial growth of GaAs on Si substrates is a promising way to integrate the attractiveness of GaAs devices with the advantages of Si substrates, like wafer size, strength, large thermal conductivity, easy handling, and low cost. However, the large lattice mismatch between GaAs and Si, the large difference in thermal expansion coefficient, and the existence of anti-phase domain boundaries, are preventing the growth of high-quality GaAs films[1]. In particular, high dislocation densities ($10^7 cm^{-2}$) and tensile stresses have been observed[2] due to a 4% lattice mismatch. However, the presence of tensile stresses is contrary to what is expected from the lattice parameters. Since the lattice parameter of GaAs is larger than that of Si, GaAs should be under compressive stress if growth occurs pseudomorphically[3]. Here, we investigate the effect of the initial stages of GaAs/Si heteroepitaxy on the stress in the GaAs layers.

2. Experimental

GaAs films were grown in a conventional molecular beam epitaxy (MBE) apparatus. The Si substrates were 2-inch-diameter wafers, oriented to within ±1° from the (001) plane and were 300 μm thick. The effusion cells with pyrolytic boron nitride (PBN) crucibles containing Ga, Si, and As were resistively heated. The shutter open duration for the Ga beam was monitored by reflection high-energy electron diffraction (RHEED) oscillations. The stress in the GaAs epitaxial layers on Si was evaluated by a stress gauge and a double-crystal X-ray diffractometer.

3. Results and Discussion

3.1 Initial stage of GaAs growth on Si substrates

A GaAs monolayer formed pseudomorphically on a Si substrate by the procedure reflected in Figure 1. The RHEED patterns observed at substrate temperatures marked A to F were also shown in the figure. A Si (001) substrate was heat-treated at 1000°C for 20 min, resulting a

cleaned surface (A). Next, amorphous Ga and As were deposited at room temperature (B). The Si substrate was heated gradually to facilitate solid-phase epitaxial growth. A streak pattern, indicating uniform layer growth appeared at substrate temperatures around 350 °C (C). As the substrate temperature was further increased to about 450 °C, spot indicating island-like growths appeared (D). An integral order pattern with a 1/2-order streak pattern appeared at substrate temperature around 600°C(E). When the substrate temperature reached 720 °C, the GaAs monolayer was completely reevaporated from the Si substrate, and the initial RHEED pattern for the Si substrate reappeared (F). We thus conclude that the temperature for pseudomorphic rearrangement of the GaAs monolayer by a type of solid-phase epitaxy was between 200°C and 450 °C.

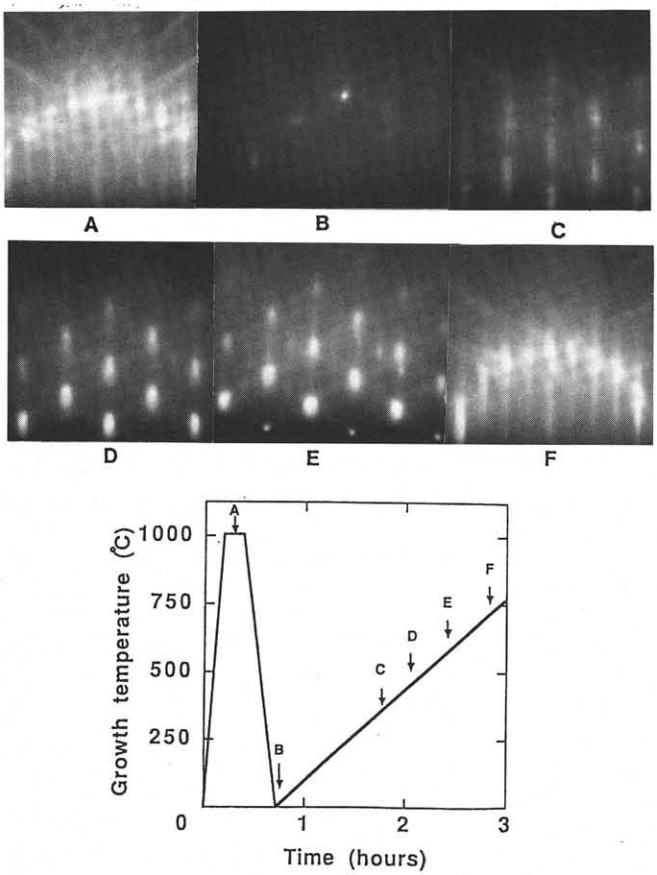

Fig. 1. RHEED patterns and the growth temperature profile for a GaAs epitaxial layer on a Si substrate.

3.2 Initial stage of Si growth on GaAs substrates

The pseudomorphic monolayer growth of Si on GaAs substrates was investigated. Figure 2 shows RHEED patterns and RHEED intensity oscillations for a Si epitaxial layer grown on a GaAs substrate at 580 °C. After a 20-second Si irradiation, a streaky RHEED pattern was observed, indicating the layer-by-layer growth of Si. This was also confirmed by the RHEED oscillation shown in the figure. However, RHEED intensity oscillations became undetectable after 2 min because of the spotty transmission nature of the RHEED pattern. We can monitore the shutter opened durations for Si from RHEED oscillation period, assuming one RHEED intensity oscillation cycle yields the biatomic layer mode[4].

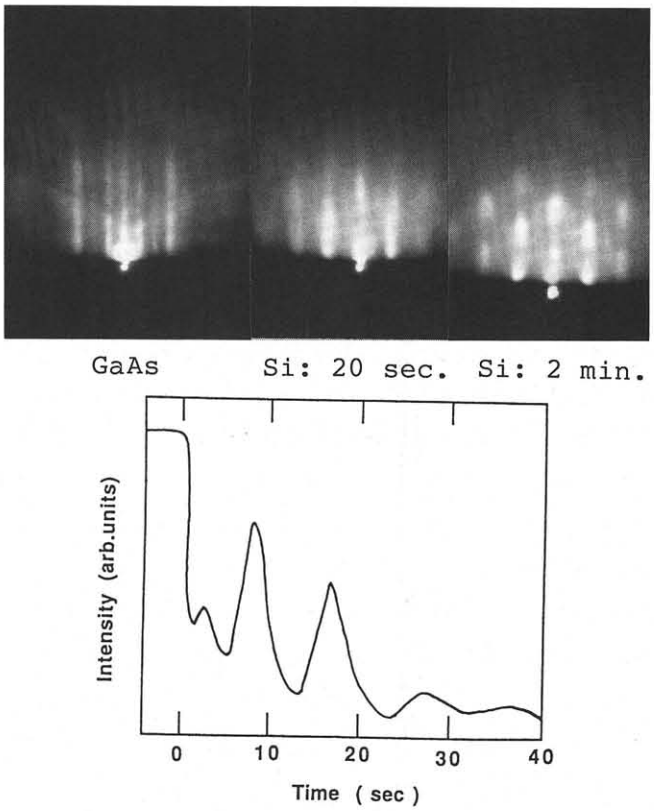

Fig. 2. RHEED patterns and RHEED intensity oscillations for a Si epitaxial layer on a GaAs substrate.

3.3 Two-step growth for Si-GaAs superlattice

We applied the Si-GaAs superlattice buffer layer to the growth of thick GaAs heteroepitaxial layers by the two-step growth technique.

Figure 3 shows the growth temperature profiles for the samples prepared for this study. After a Si (001) substrate was heat treated at 1000°C for 20 min, a single monolayer of GaAs, monitored by RHEED intensity oscillations, was irradiated at room temperature. First, the Si substrate was heated to 200°C to facilitate solid-phase epitaxial growth under an As flux. Next, the substrate temperature was maintained at 200°C, and the biatomic layer Si beam, again monitored by RHEED intensity oscillations, was irradiated for one minute after the As beam was turned off. The Si substrate temperature was lowered again. Another single monolayer of GaAs was deposited at room temperature, and the substrate was heated to 200°C. After the growth of Si-GaAs superlattice buffer, a thick GaAs layer (about 2 μm) was deposited at substrate temperatures from 200°C to 680°C by the two-step growth process.

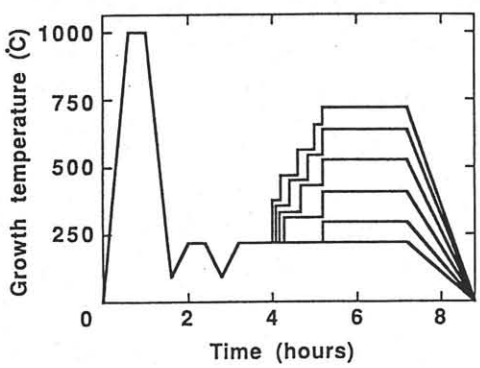

Fig. 3. Growth temperature profiles for the two-step growth including a Si-GaAs superlattice buffer.

3.4 Dependence of stress on substrate temperature

The stress in the GaAs layers was evaluated by a stress gauge and a double-crystal X-ray diffractometer.

Figure 4 graphs the dependence of the stress on the substrate temperatures. Solid circles indicate stress T obtained from the stress gauge measurements using the equation below[5],

$$T = \frac{(d_{Si})^2}{6\,R\,d_{GaAs}} \cdot \frac{E_{Si}}{(1-\nu_{Si})}, \qquad (2)$$

where E_{Si} is Young's modulus of Si, d_{Si} and d_{GaAs} are the thickness of the Si and GaAs layers, ν_{Si} is the Poisson's ratio of Si, and R is the radius of curvature. Open circles indicate the results calculated from the lattice constant[6],

$$T = \frac{E_{GaAs}}{2\,\nu_{GaAs}} \cdot \frac{a_0 - a_\perp}{a_0}, \qquad (3)$$

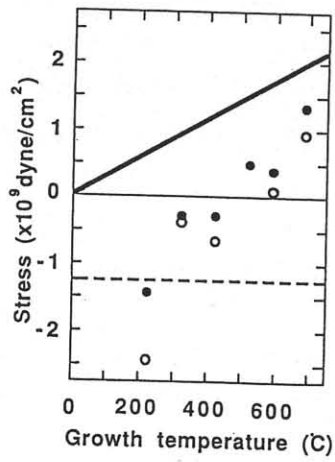

Fig. 4. Dependence of the stress on the substrate temperatures and the results of analysis of stress and its dependence on growth temperatures.

where E_{GaAs} is Young's modulus of GaAs, ν_{GaAs} is Poisson's ratio of GaAs, and a_0 is the lattice constant in bulk GaAs, $a_\perp$ is the lattice constant for GaAs on Si in a direction perpendicular to the Si substrate. At a substrate temperature of 500 °C, the GaAs lattice constant approached that of the unstressed sample (0.56535 nm). The tensile stress was observed at temperatures greater than 520 °C; the substrate bowed inward. Compressive stresses were observed at temperatures lower than 420 °C; the substrate bowed outward. The dependence of stress on temperature can be explained by considering thermal expansion difference and lattice miamatch between GaAs and Si. The stress, caused by thermal coefficient of expansion mismatch is given by [7].

$$S = E_{GaAs} (\alpha_{GaAs} - \alpha_{Si}) \Delta T, \quad (4)$$

where α_{GaAs} and α_{Si} are the coefficients of thermal expansion of GaAs and Si, and ΔT is the difference between growth and room temperatures. The solid line in Figure 4 represents the theoretical curve calculated by equation (4). The dotted line in Figure 4 indicates the difference between the calculated value (solid line) and the value measured from the radius of curvature (solid circle). It is estimated from Figure 4 that a nearly constant compressive stress is generated over the entire range of substrate temperatures used in this experiment. Assuming that the stress resulting from lattice constant mismatch is 1.25×10^9 dyne/cm^2, the strain is 8×10^{-4}. The initial stage of Si-GaAs superlattice growth is critical to reduce the stress in thick GaAs films grown at a high temperature of 500 °C.

4. Conclusion

The Si-GaAs superlattice buffer was grown on Si substrates at temperatures of 200 °C. This Si-GaAs superlattice growth technique was applied to the growth of thick GaAs films with the two-step growth technique. Stress-free, 2 μm-thick GaAs films were obtained at around 500 °C. This is explained by a balance of the tensile stress due to the thermal expansion mismatch and the compressive stress due to a residual lattice constant mismatch.

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