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Improvement of SiO_2/Si Interface Properties by Fluorine Implantation

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Introduction: One of the key issues in processing technology for deep-submicron MOS VLSIs is to develop reliable SiO_2/Si interfaces. Recent studies suggest that fluorine incorporation during oxidation improves SiO_2/Si interface properties[1]. In this paper, a new effective method of fluorine introduction into SiO_2/Si interface using ion implantation is presented. This will significantly reduce pn-junction leakage current and will improve MOSFET hot-carrier immunity.

Experimental: The method used was as follows: (1) F ion implantation into the gate poly-Si and source/drain doped regions; (2) subsequent heating (950 ℃, 10 min) to anneal implant damage and to drive some of the F atoms to the adjacent SiO_2/Si interfaces.

Results: The initial interface state density at mid-gap decreased significantly to the detectable limit ($\sim 1\times10^{9}/cm^2/eV$) when the F implant dose was adequate (Fig. 1). On the other hand, the fixed charge density, and consequently the threshold voltage, remained unchanged except for an F dose that was too high (Fig. 1). This reduction in interface state density correlates very well with the dramatic reduction in the junction leakage current. A typical result for a gate-controlled junction diode clearly indicates that leakage current due to carrier recombination at the interface decreased by a factor of three (Fig. 2).

In addition, stability of the fluorine introduced SiO_2/Si interface was confirmed. Increases in the interface state density induced by Fowler-Nordheim electron injection were notably suppressed (Fig. 3). Moreover, MOSFET hot-carrier immunity was improved by 3 times in the case of $\sim 2\times10^{15}$ F ions/cm^2 (Fig. 4).

It must be noted here that there is an optimal range of the F implant dose. In fact, F doses that were too high resulted in degradation of hot-carrier immunity as well as junction characteristics. The amount of F was controlled very well to maximize the effect of fluorine incorporation. From this point of view, the implantation technique is a promising method.

Conclusion: An effective method to prepare high quality SiO_2/Si interfaces has been demonstrated. It also sheds light on a way to improve junction characteristics and device reliability which are indispensable to further device miniaturization.

Reference: 1) E.F. da Silva et al., IEEE Trans Nucl. Sci., NS-34 1190 (1987)

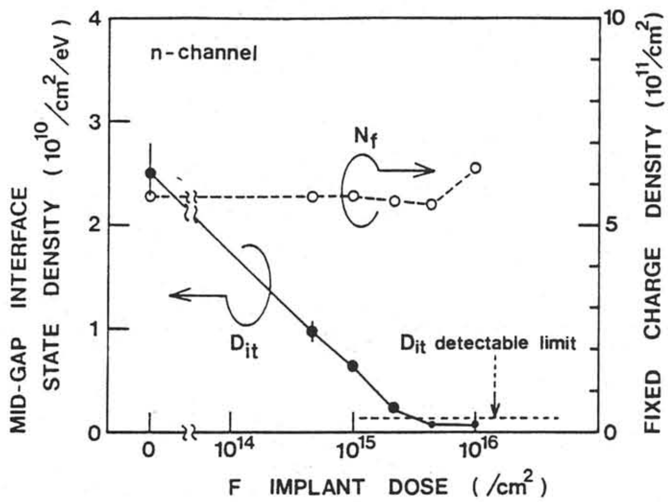

Fig. 1 Fluorine implant effect on interface state density (Dit) and fixed charge density (Nf) of MOS capacitors.
(Substrate: 10Ω·cm, p-type, (100) Si, SiO_2: 16nm thickness (wet oxidation at 850℃))

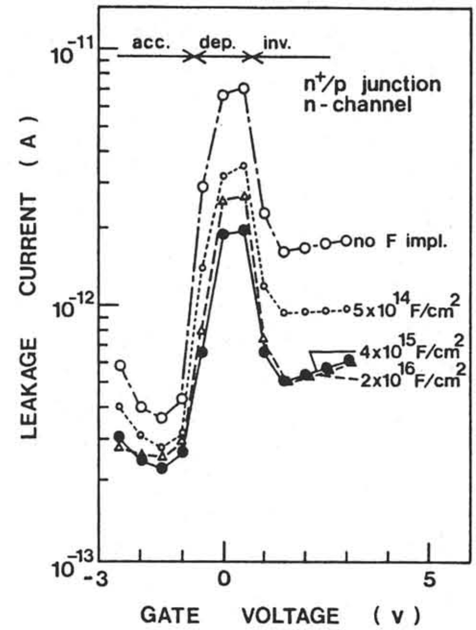

Fig. 2 Reduction in gate-controlled n^+/p junction diode leakage current by F incorporation.
(Junction area: 4×10^{-4} cm², Junction perimeter: 1cm, Gate area: 3×10^{-4} cm², Reverse bias: 1V)

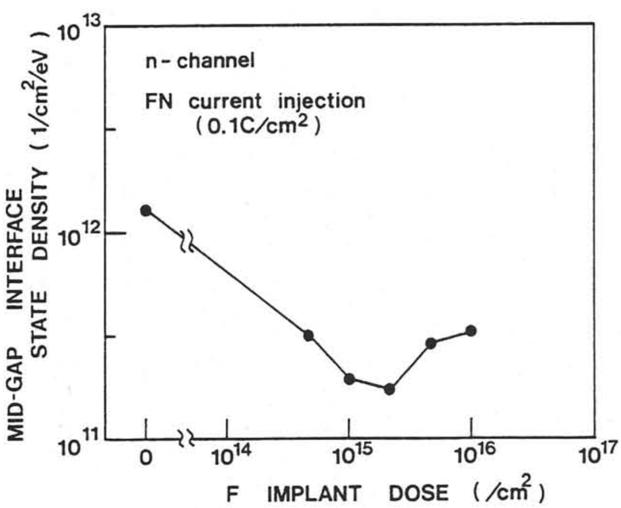

Fig. 3 Minimization of Fowler-Nordheim current stress induced interface state density by F implantation.
(Electron injection from substrate to gate through 16nm SiO_2)

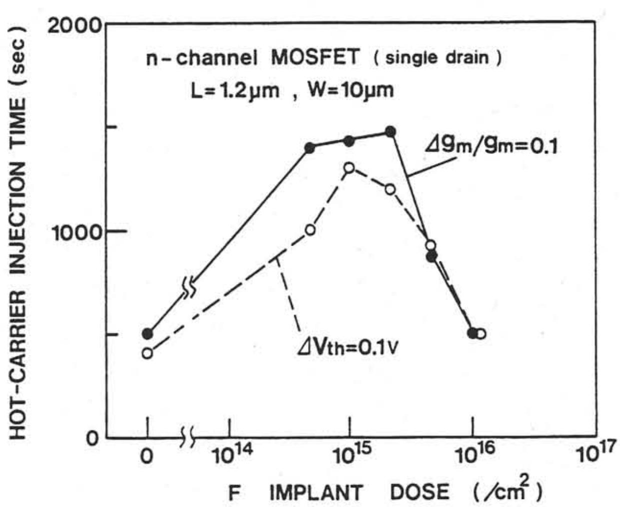

Fig. 4 MOSFET hot-carrier immunity improvement by F implantation as evaluated in terms of hot-carrier injection time causing 10% variation in channel conductance (gm) and 0.1V shift in threshold voltage (Vth).
(Gate bias: 3V, Source-drain bias: 7V)