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A Novel Device Structure for Latch-up Free VLSI CMOS Circuits

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Abstract: A new concept, where well- and substrate- contacts are replaced by diodes, provides latch-up free CMOS circuit operation without degrading the MOS device parameters. For the 4 Megabit 0.9 µm n-well bulk CMOS technology with VBB-generator, the well contact is substituted by a buried poly-Si diode. Compared to conventional CMOS, no additional area is needed.

1. Theory of Operation

Many concepts have been presented in the past that claimed to provide latch-up free CMOS circuits. But a high price had to be paid; i.e. expensive (epilayer [1]) and complicated (Schottky PMOS [2]) technologies or increased die size (additional guardrings [3], other design measures [4]). A new idea [5], combining the good static latch-up hardness of floating well concepts [4] and the low transient latch-up suszeptibility of conventional CMOS leads to a simple unique solution without degrading MOS device performance. The principle of operation is discussed in detail in [5].

Fig.1a shows the cross section of this new CMOS structure. If compared to conventional CMOS, no additional area is needed for this structure. Fig.1b shows the equivalent circuit of a CMOS stage, where the substrate and well contacts are replaced by diodes. The n-well (or n-substrate) of the PMOS device is connected with the cathode of diode D1 to VCC. The p-substrate (or p-well) of the NMOS device is connected with the anode of diode D2 to VSS. There is no significant increase of substrate and well shunt resistances. The MOS device performance is not degraded.

In the case of power-on, majority carriers only can flow out of the well and out of the substrate. Proper biasing of well and substrate is achieved by threshold voltages of the additional diodes lower than the threshold voltages of the parasitic p^+n and n^+p diodes.

Under static conditions only the small leakage current of the p-n junctions will act as a base current for the parasitic bipolar transistors.

2. Technology and Diode Device Features

Basis for the new device structure is the 4M DRAM 0.9µm n-well CMOS technology [6]. In p^+ regions (p^+ source/drain of the p-channel MOS) the outdiffusion of As out of the As doped poly-Si forms a n^+p^+ junction. Fig.2 shows a microphotograph of a cross section of the new poly-Si diode. The n^+ outdiffusion is 0.1µm into the 0.6µm deep p^+ diffusion region. Fig.3 shows the I/V characteristics of the device.

3. Latch-up Measurements

The latch-up hardness of the new concept using poly-Si diodes is compared to conventional CMOS and floating well CMOS.

3.1 Static Latch-up Behaviour

To characterize the static latch-up behaviour of the CMOS stage (VCC=5V; Fig.4; results in Tab.1) a current is forced into the output pin. The PMOS and NMOS are in the OFF state. For positive currents at the output pin, the conventional CMOS structure latches at VCC+0.7V (V_{DO}=5.7V) at a trigger current of only $I_{DO} \leq 8mA$. The floating well concept and the new concept with the poly-Si diode are latch-up free for voltages $V_{DO} > 8V$. For negative currents at the output pin, all 3 concepts are latch-up free because of the use of a VBB-generator. The trigger currents I_{DO} are greater than 100mA at a trigger voltage V_{DO}=-3.4V.

3.2 Transient Latch-up Behaviour

The power-on latch-up hardness is investigated with a VCC=7V/2ns ramp rate and a DC voltage source at the DO pin (Fig.5; results Tab.2). The power-on latch-up hardness of the conventional CMOS stage is taken as a reference. The floating well concept offers some advantages for positive DC voltages at the DO pin while for negative voltages V_{DO} the latch-up hardness is worse. A real improvement is obtained for the stage with the poly-Si diode, where the structure is latch-up free for voltages $V_{DO} \geq -1V$ and $V_{DO} \leq 5.2$ V.

4. Conclusion

The new concept with poly diodes instead of conventional substrate and well contacts provides latch-up free CMOS circuits with additional benefits as easy layout and reduced die size if compared to guardring technologies. The fabrication of the poly-Si diodes can easily be implemented in the 4M DRAM 0.9µm n-well bulk CMOS process.

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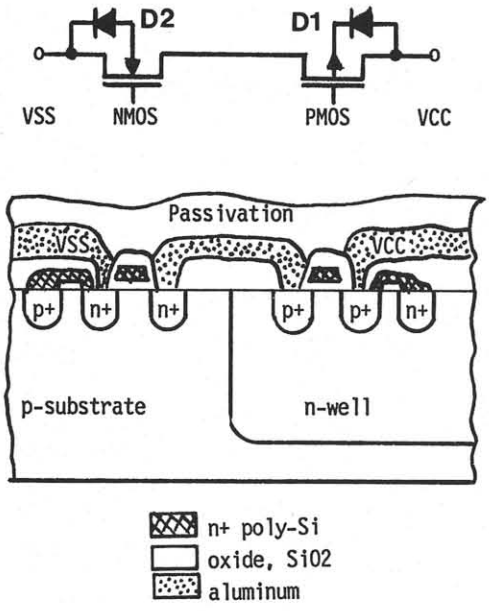

Fig.1: CMOS output stage with additional diodes.Cross section a.) and equivalent circuit b.) of the proposed structure with poly-Si diodes instead of substrate and well contacts.

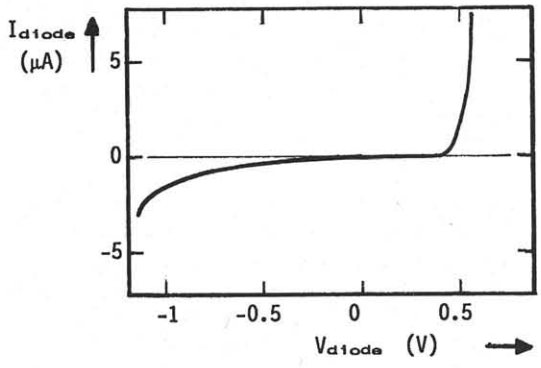

Fig.3: I/V characteristics of the poly-Si diode.

buffer design	trigger current/voltage
A well on VCC=conventional CMOS	+8mA / 5.7V no LU at -100mA / -3.4V
B floating well	no LU at V_{DO} > 8V no LU at -100mA / -3.4V
C poly-Si diode	no LU at V_{DO} > 8V no LU at -100mA / -3.4V

Tab.1: DC latch-up trigger currents/voltages for different CMOS buffers. W/L=400µm/1.1µm and W/L=600µm/1.1µm for NMOST and PMOST, respectively. VCC = 5 V, LU = latch-up.

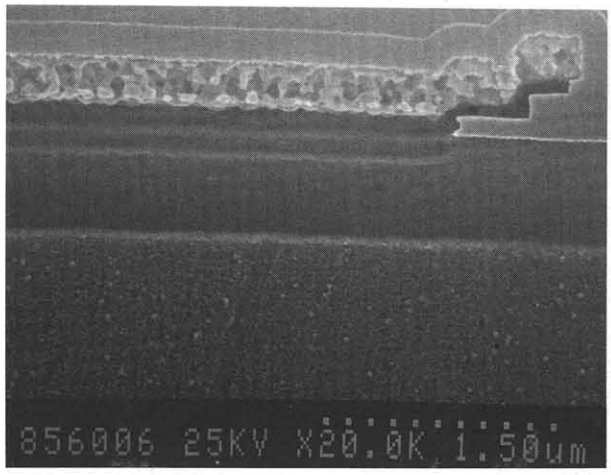

Fig.2: SEM - Microphotograph of the poly-Si diode (Cross section).

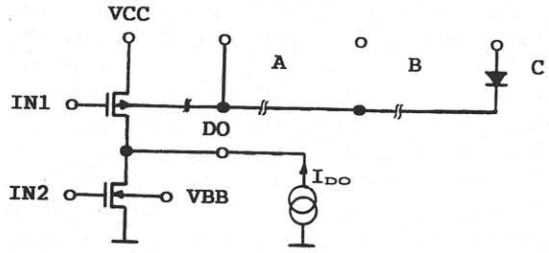

Fig.4: Measurement setup for static (DC) latch-up characterization.

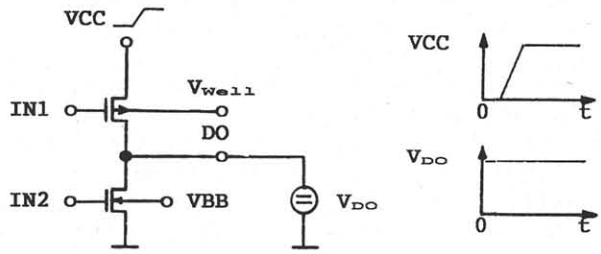

Fig.5: Measurement setup for power-on latch-up characterization (worst case condition).

buffer design	voltage on DO pin
A well on VCC=conventional CMOS	≤ -0.34V ≥ +1.7V
B floating well	≤ -0.29V > 8V
C poly-Si diode	≤ -1V ≥ +5.2V

Tab.2: Power-on latch-up trigger currents/voltages for different CMOS buffers.W/L=400µm/1.1µm and W/L=600µm/1.1µm for NMOST and PMOST, respectively. Ramp rate VCC=7V/2ns, LU=latch-up.