

Performance Improvement in Fully Depleted Thin Film SOI MOSFETs

Y.Yamaguchi, H.Miyatake, S.Kusunoki, T.Nishimura and Y.Akasaka
LSI Research and Development Laboratory
Mitsubishi Electric Corporation
4-1 Mizuhara Itami, 664 Japan

It has been reported that MOSFETs fabricated in thin SOI structure (MOSFET/T-SOI) had several significant advantages when the SOI layer was fully depleted.¹⁻²⁾ Especially, the theoretical study for the increase of carrier mobilities and the subsequent increase of saturation current are very attractive from the view point of device performance. In this paper we investigated the thin SOI nature for the electrical characteristics by comparing the fully-depleted thin film SOI/MOSFETs with partially-depleted cases by applying the back gate biases.

MOSFETs/T-SOI were fabricated in SIMOX films which were formed by oxygen ion implantation into p-type (100) Si with a dose of $2.2 \times 10^{18}/\text{cm}^2$ and at an energy of 180keV at substrate temperature of 530 °C. The wafers were annealed at 1180°C for 6 hours in N₂. The devices were fabricated by conventional CMOS processing with p⁺-polysilicon gate for controlling the threshold voltage (V_T) and the thickness of finished SOI layer became 120nm.

Fig.1-(a) and -(b) show the typical I_D - V_D characteristics of fully-depleted nch-MOSFETs/T-SOI and the partially-depleted case by applying the back gate bias of -20V, respectively. No kink effect was observed in the fully-depleted MOSFET, while for partially-depleted case, the kink was apparently observed because of appearance of neutral region. Fig.2 shows the measured carrier mobility of nch-MOSFET/T-SOI as a function of back gate bias voltage. No significant change was seen between a fully-depleted and a partially-depleted mode. This indicates that the change of the average electric field in a vertical direction due to T-SOI structure has no significant effect on the carrier mobility.

Fig.3 shows the saturation voltages (V_{SAT}) in a fully-depleted and partially depleted nch-MOSFETs/T-SOI as a function of ($V_G - V_T$) which is the effective gate voltage for the inversion layer. For a fully-depleted mode, the value of the V_{SAT} became almost the same as that of ($V_G - V_T$) and this indicates that the I_D - V_D characteristics of the fully-depleted MOSFET/T-SOI in a saturation region is very close to the ideal characteristics. But for partially-depleted modes, V_{SAT} became smaller than that in a fully-depleted mode. From these data, it is considered that the mobile charge is more effectively generated in an inversion layer for a fully depleted mode due to limited number of space charge as compared with the partially-depleted cases, and results in a higher saturation voltage and also a higher drain current for a fully-depleted case as shown in Fig.4.

In conclusion, we investigated the T-SOI nature for the I_D - V_D characteristics of MOSFETs, and well demonstrated the feature of the increase of saturation current in fully-depleted MOSFETs/T-SOI.

- 1) J. P. Colinge, IEEE, EDL-7, 244 (1986)
- 2) M. Yoshimi et al, Tech. Dig. of IEDM 1987, 640

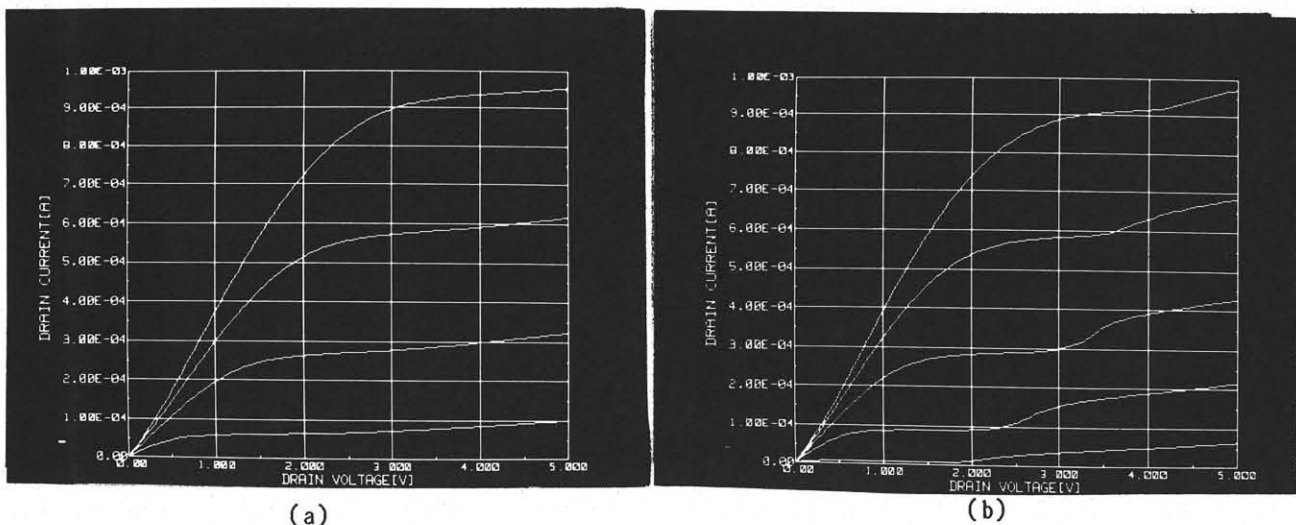


Fig.1 I_D - V_D characteristics of (a) fully-depleted ($V_{BACK}=0V$, $V_G=0\sim 5V$) and (b) partially-depleted ($V_{BACK}=-20V$, $V_G=0\sim 6V$) n-ch MOSFETs/T-SOI ($L=2\mu m$, $W=10\mu m$)

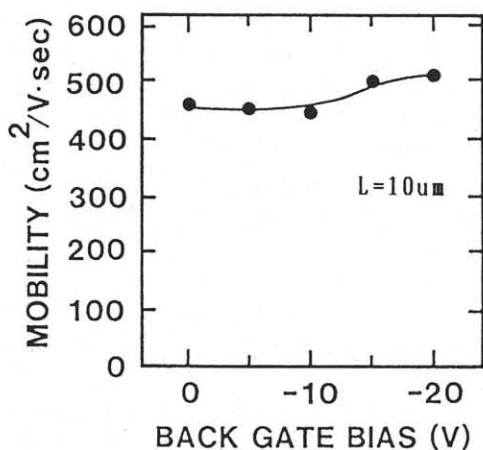


Fig.2 Measured carrier mobility of n-ch MOSFETs/T-SOI as a function of back gate bias ($L=10\mu m$)

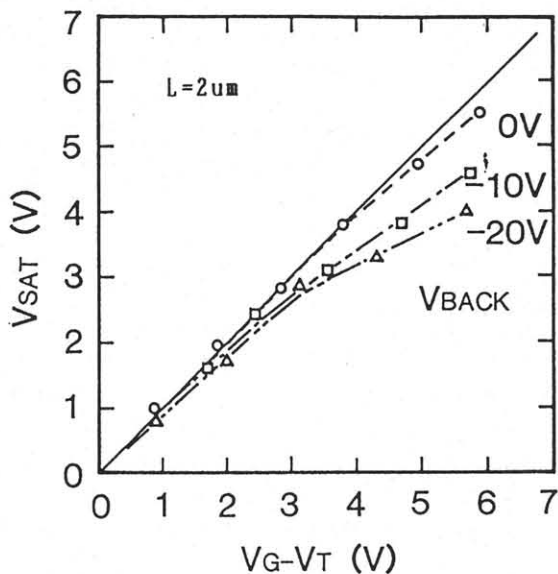


Fig.3 Saturation voltages of a fully-depleted ($V_{BACK}=0V$) and partially-depleted ($V_{BACK}=-10$ and $-20V$) n-ch MOSFETs/T-SOI as function of $V_G - V_T$ ($L=2\mu m$)

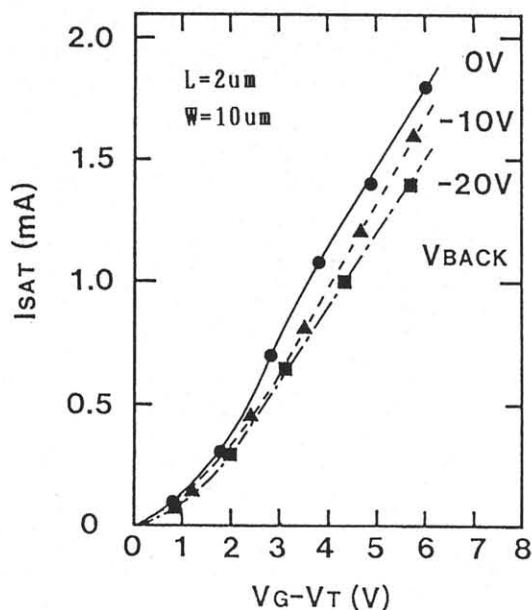


Fig.4 Saturation current of a fully-depleted ($V_{BACK}=0V$) and partially-depleted ($V_{BACK}=-10$ and $-20V$) n-ch MOSFETs/T-SOI as function of $V_G - V_T$ ($L=2\mu m$)