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Low Temperature Pseudo HBT Utilizing Bandgap Narrowing Effect

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I. INTRODUCTION

Low-temperature operation of Si bipolar transistor, which long has been considered to be useless due to its poor current gain, has received attention in recent years due to its potential application to low-temperature BiCMOS. Previous work showed bipolar transistor operates even at liquid nitrogen temperature with sufficiently high current gain and almost the same speed as room temperature(1, 2, 3) by employing some design modifications. However, for BiCMOS application bipolar transistor should have superior f_T to room temperature, unless the speed advantage of BiCMOS over pure CMOS at low temperatures degrades severely compared with room temperature. This paper proposes and characterizes a new Si bipolar structure, named low-temperature pseudo HBT, using a new experimental method and a new device simulator. The transistor has lightly-doped emitter and heavily-doped base, which modulates the spacial dependence of bandgap into HBT-like profile due to bandgap narrowing effect, providing the potential of very high speed and good scalability.

II. LOW-TEMPERATURE PSEUDO HBT

Proposed Device Structure Schematic impurity profile of the proposed transistor is illustrated in Fig. 1. In the transistor bandgap narrowing is designed to be more significant in base than emitter, reducing the hole injection into the emitter. The narrowing, which is smaller than the bandgap difference in the commonly-used hetero-junction in HBT such as AlGaAs/GaAs, reduces hole injection insufficiently at room temperature, whereas it can suppress the hole injection sufficiently at low temperatures. The heavily-doped emitter and collector at both ends are employed to have good ohmic contacts.

Experiment To prove the hole blocking ability at the emitter-base junction at low temperatures, n^+np^+ vertical diodes, in which n^+ is the buried layer, are fabricated and evaluated. We employed a new method for estimating the current gain of proposed transistor using this diode. In the method the forward-bias current is measured at a specific voltage giving ideal characteristics without recombination and series resistance for various n-region concentrations N_E as shown in Fig. 2. The injected-electron current in p^+ region is expected to be independent of N_E, whereas the injected-hole current is expected to be proportional to n_{ie}^2/N_E. The less dependence of the current on the N_E in Fig. 2 at low temperatures shows that hole injection into the lightly-doped emitter is dramatically suppressed due to the hole-blocking property induced by the slight bandgap difference between emitter and base. The gradient and the intersection of the lines in Fig. 2 separate the electron current from the hole current giving Fig. 3. Fig. 3 shows the proposed transistor has large negative temperature coefficient in current gain, achieving high current gain at low temperatures.

Simulation Model To predict precisely the proposed-transistor characteristics at 50K-350K, a new simulator including carrier freezeout, Mott transition, bandgap narrowing(4), impurity-level shift due to carrier screening(5), and distinction between majority- and minority- carrier mobilities are developed. Carrier freezeout is included in the bipolar device simulator for the first time. The simulated results for the device discussed in Ref. (2) as "metal contact transistor" are shown in Fig. 4, which clarifies that good agreement with experimental results are obtained by considering carrier freezeout.

Simulated Characteristics The new transistor is found to have following remarkable features: 1)negative temperature dependences of both h_{FE} and f_T occur, which give notably high h_{FE} and f_T at low temperatures as shown in Fig. 4 and 5. This is because the hole accumulation in the lightly-doped emitter is dramatically reduced at low temperatures as shown in Fig. 6. Due to its very high current gain of this transistor, it can be also applied to an high-input-impedance analog amplifier. 2)Both of upward- and downward- operation are possible with high speed and relatively high breakdown voltage, whereas the room-temperature optimized conventional structure inevitably has poor f_T and breakdown voltage in the upward direction.

III. DEVICE PARAMETER DESIGN

Optimum design of lightly-doped-emitter concentration, and its depth is also examined as shown in Fig. 7 and 8, respectively. The major guidelines clarified by this study are: 1)The emitter concentration should exceed Mott-transition concentration 3.0×10^{18} cm^{-3} to avoid carrier freezeout both in the emitter and in compensating donor in the base as shown in Fig. 7. 2)Lightly-doped-emitter depth is long enough when it is only 20nm as shown in Fig. 8 ; therefore, the proposed transistor operates advantageously when it is considerably scaled down.

IV. CONCLUSION

The proposed pseudo heterojunction-bipolar transistor is found to operate about 2-3 times faster than room-temperature optimized conventional transistor, which can realize ultra-fast-low-temperature BiCMOS.

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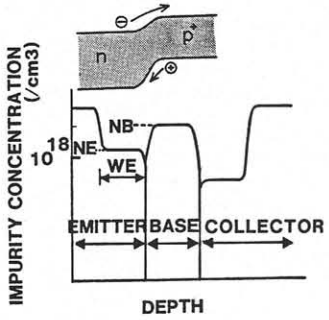

Fig. 1. Basic impurity profile of pseudo-HBT

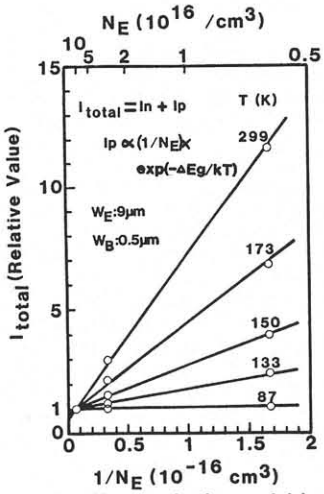

Fig. 2 Measured forward-bias current vs. "lightly-doped-emitter" concentration for n$^+$np$^+$ diode. The measured diode has ideal exponential IV characteristics with n-value of 1.004-1.03 in the temperature range of 120K-300K and 1.03-1.10 in the range of 87K-120K. N_{Emax} = 1.0 x 10^{20} cm^{-3}. The measured current is from 10nA to 1μA.

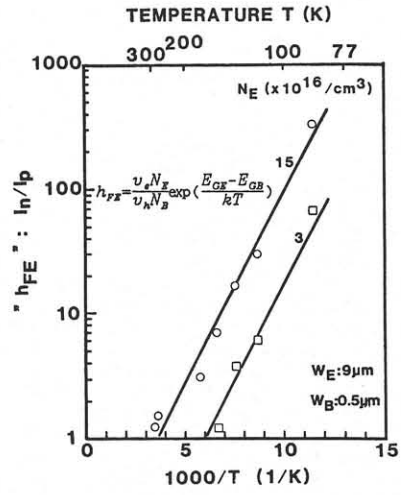

Fig. 3 Current gain vs. inverse temperature obtained using the measured gradient and intersection of the lines in Fig. 2.

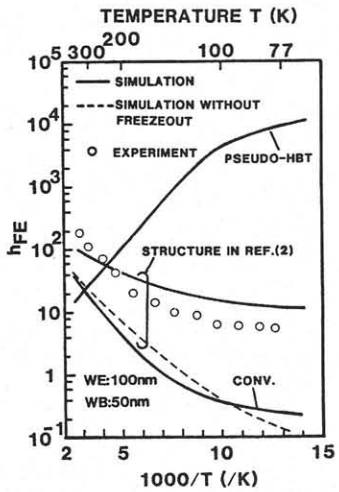

Fig. 4. Current gain vs. inverse temperature for pseudo-HBT, conventional transistor, and "Optimized metal contact transistor" from Ref. (2). Pseudo-HBT has 3.0 x 10^{18} cm^{-3} emitter and collector and 3.0 x 10^{19} cm^{-3} base. Conventional transistor has 1.0 x 10^{20} cm^{-3} emitter, and 3.0 x 10^{18} cm^{-3} base.

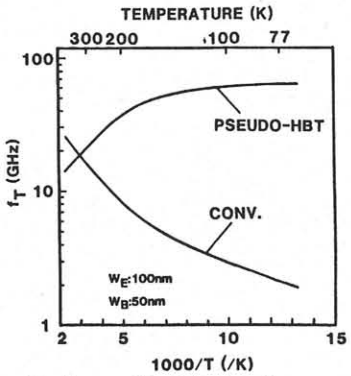

Fig. 5. Simulated f_T vs. inverse temperature for pseudo-HBT and conventional transistor. The impurity profile is the same as Fig. 4.

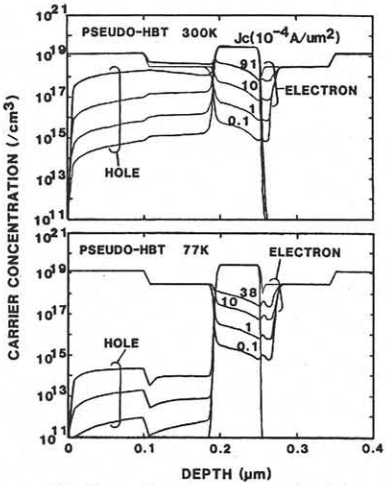

Fig. 6. Carrier concentration vs. depth for pseudo-HBT.

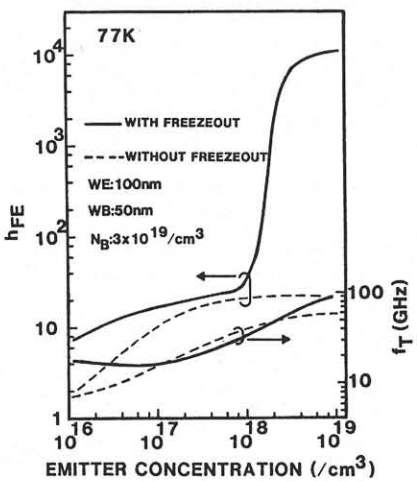

Fig. 7. Simulated h_{FE} and f_T vs. emitter concentration at 77K. Freezeout in base-tail region improves current gain.

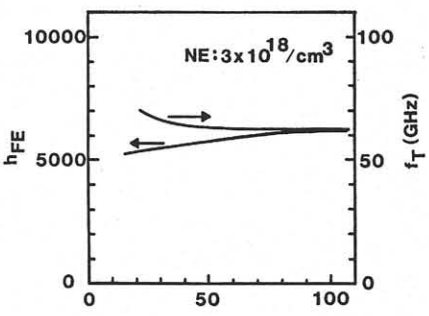

Fig. 8. Simulated h_{FE} and f_T vs. lightly-doped-emitter depth.