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Low Temperature Thin Film Transistor Fabrication Using a Polycrystalline Silicon Film Formed from a Fluorinated Silicon Film

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Polycrystalline silicon thin-film transistors (poly-Si TFTs) have attractive potential for realizing large-area active-matrix-addressed liquid crystal displays (LCDs) with on-glass peripheral circuits because of their high field-effect mobility.[1] Low-cost glass substrates in such LCDs need low-temperature fabricated TFTs with high field-effect mobility. Recently, extremely low-temperature (200°C) epitaxial growth of Si-on-single-Si substrates by PCVD using SiH_2F_2, SiH_4 and H_2 mixing gases has been reported.[2] This implies the possibility of forming a high-quality poly-Si film on an amorphous substrate at a lower temperature than conventional methods. We have fabricated a TFT with high field-effect mobility at a low-temperature using a poly-Si film formed from a fluorinated Si film.

The poly-Si films were formed by recrystallization annealing of Si films deposited on quartz substrates at 200°C by PCVD using a mixture of SiH_2F_2, SiH_4 and H_2. The SiH_2F_2 flow rate was varied from 0 to 25 sccm because it was expected to affect the film crystalinity. The flow rates of SiH_4 and H_2 were constant. The film thickness was 150 nm. The recrystallization annealing was carried out at 600°C for 24 hours in an N_2 atmosphere.

The SiH_2F_2 flow rate dependence of average grain size in annealed films is shown in Fig. 1. The average grain size was measured from TEM dark field images. The grain size increases with increasing SiH_2F_2 flow rate and shows a maximum value of 230 nm at 20 sccm. The SiH_2F_2 flow rate dependence of the surface crystalline fraction in as-deposited and annealed films is shown in Fig. 2. The surface crystalline fraction was obtained from UV reflectance measurements. The crystalline fraction in annealed films is greater than 70% regardless of the SiH_2F_2 flow rate. However, the fraction in as-deposited films decreases with increasing SiH_2F_2 flow rate and drops below 5% when the rate is greater than 10 sccm. TEM dark field images of as-deposited films show a microcrystalline poly-Si structure when SiH_2F_2 flow rate is lower than 10 sccm. On the other hand, they show a microcrystalline amorphous Si structure when SiH_2F_2 flow rate is 10 sccm or greater. These results suggest that adding SiH_2F_2 gas decreases the nuclear site density. It is considered that the recrystallization proceeds from the nuclear site until the boundaries of all neighbouring grains come to face each other.

TFTs were fabricated using the poly-Si films described above. A schematic diagram of the TFT is shown in Fig. 3. To form a good quality gate-insulator film at low-temperature, a sputtered SiO_2[3] film deposited at 200°C was used. The source and drain were formed by phosphorous ion implantation and then annealed at 600°C. The relationship between field-effect mobility and poly-Si grain size is shown in Fig. 4. Field effect mobility sharply increases with increasing grain size as determined by the SiH_2F_2

flow rate. The maximum value is 17 cm^2/Vs, which is more than three times that of a TFT using a conventional CVD poly-Si film deposited at 600°C.

In conclusion, a new poly-Si film formation method using fluorinated Si film has been developed to fabricate TFTs by a process with a maximum temperature of 600°C. The field-effect mobility of the TFT was 17 cm^2/Vs. We believe that this method can produce high-mobility poly-Si TFTs on low-cost glass substrates.

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2) K. Nagamine, A. Yamada, M. Konagai and K. Takahashi: Jpn. Appl. Phys. **26** (1987) L471.
3) S. Suyama, A. Okamoto and T. Serikawa: IEEE Trans. Electron Devices **ED-34** (1987) 2124.

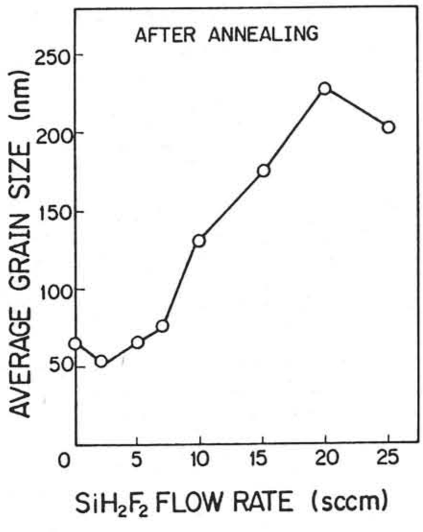

Fig. 1. SiH_2F_2 flow rate dependence of average grain size in annealed films.

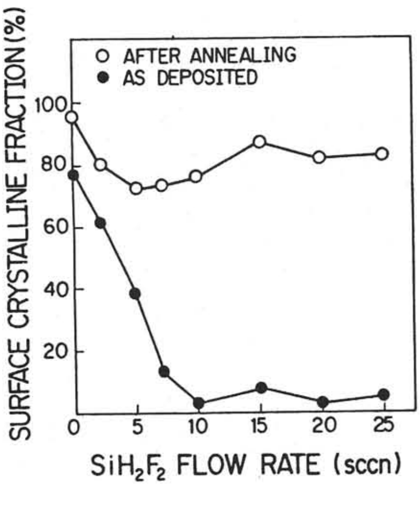

Fig. 2. SiH_2F_2 flow rate dependence of the surface crystalline fraction in as-deposited and annealed films.

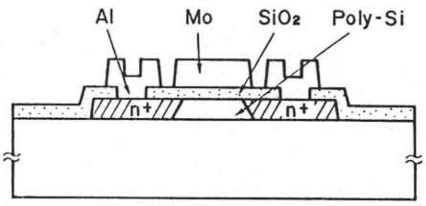

Fig. 3. Schematic diagram of the TFT.

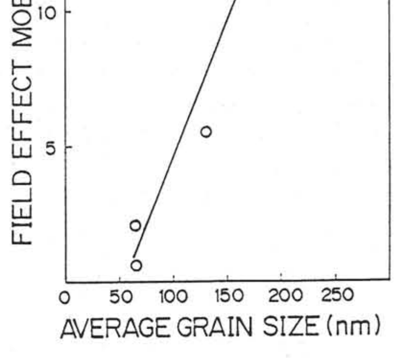

Fig. 4. Relationship between field-effect mobility and poly-Si grain size.