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A High Speed 1-kbit Variable Threshold Josephson RAM Chip

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This paper reports a high speed 1-kbit Josephson RAM(Random Access Memory) chip integrating variable threshold memory cells[1].

A block diagram of a 256 x 4-bit(1-kbit) RAM is shown in Fig.1. The memory plane is organized into four blocks, each with 64 rows and 4 columns. The variable threshold memory cell which has been proposed and investigated[2] has an equivalent circuit of asymmetric dc SQUID(Superconducting Quantum Interference Device) as shown in Fig.2. The cell has a simple structure in comparison with other Josephson memory cells. The present cell is two times smaller than the conventional ones[3,4,5]. This is very important to achieve a high performance Josephson memory, not only for the storage capacity but also for the access time.

The address decoder circuit consists of OR-gates and INVERT-gates, instead of AND-gate used in the conventional one. Therefore this circuitry gives a small area and a fast operating speed. One column is driven by a pair of set-reset gates with a feedback signal from the sense gate to achieve an NDRO(Non-Destructive Read Out) operation. By introducing a two phase unipolar power supply it is realized to operate the RAM chip in a pipe-line way which makes the cycle time shorter than that in a single phase or a dc power supply systems. All of the inputs are set in the active cycles of the power of phase 1 before the power of phase 2 rises up. The positive and the negative signals are made at the input buffer gates. These all peripheral circuits consist of a 4JL-gate family[6].

A photomicrograph of the 1-kbit RAM is shown in Fig.3. The chip has been fabricated based on the Nb/Al-oxide/Nb junction technology with 3-μm design rule[7]. The cell size is 30μm x 72μm. Whole circuits are integrated in an area of 3.3mm square on the chip.

All operating function tests were carried out in liquid He. Figure 4 shows a result of repeatable operations of write"1", read, write"0" and read sequence for all bits. Marks"o" in the figure show correct-responding bits to the sequential operation. "x" indicates the location of the cell which responds incorrectly. More than 90% of the cells showed their right response. From high speed measurements, the critical delay time of the decoder and the memory plane were obtained to be 150ps and 350ps, respectively.

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[2]I.Kurosawa et al.,*Ext.Abst.16th SSDM*,p619(1984).
[3]M.Yamamoto et al.,*IEEE Electron Device Lett.*,**EDL-4**,p150(1983).
[4]W.H.Henkels et al.,*J.Appl.Phys.*,**58**,p2371(1985).
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[7]H.Nakagawa et al.,*Jpn.J.Appl.Phys.*,**25**,pL70(1985).

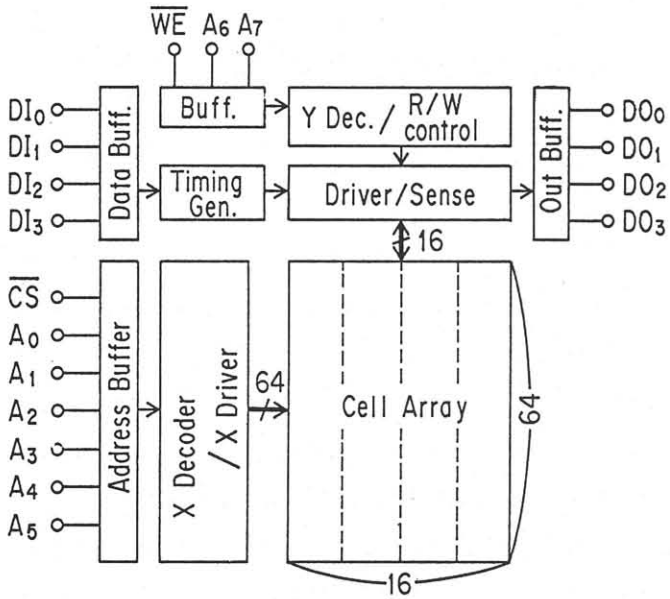

Fig.1 Block diagram of the 1-kbit Josephson RAM.

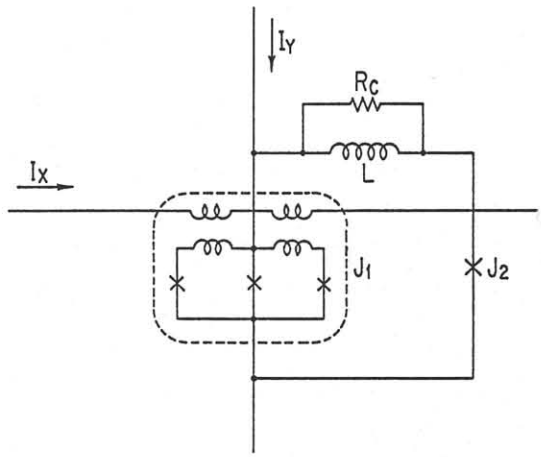

Fig.2 The variable threshold memory cell.

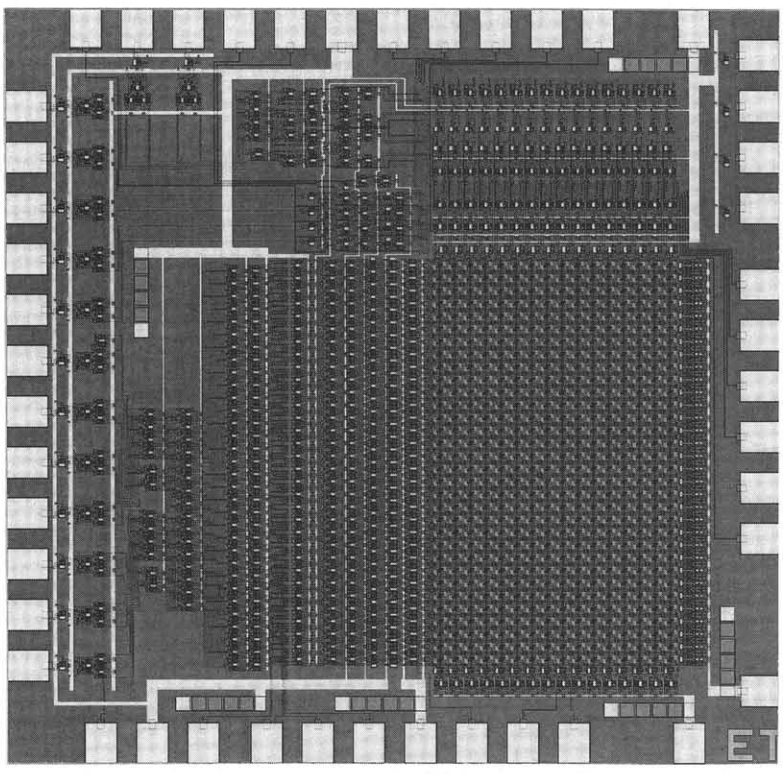

Fig.3 Photomicrograph of the 1-kbit Josephson RAM.

	bit1-4	bit5-8	bit9-12	bit13-16
1	XOXO	OOOO	OOOO	OOXO
2	XOXO	OOXO	OOOO	OOOO
3	OOOO	OOOO	OOOO	OOOO
4	OOOO	OOOO	OOOO	OOOO
5	OOXO	OOOO	OOOO	OOOO
6	XOOO	OOXO	OOOO	OOOO
7	OOOO	OOOO	OOOO	OOOO
8	OOOO	OOOO	OOOO	OOOO
9	OOOO	OOOO	XOOO	OOOO
10	OOOO	OOXO	OOOO	OOOO
11	OOOO	OOOO	OOOO	OOOO
12	OOOO	OOOO	OOOO	OXOO
13	OOOO	OOOO	XOOO	OOOO
14	OOOO	OOXO	OOOO	OOOO
15	OOOO	OOOO	OOOO	OOOO
16	OOOO	OOOO	OOOO	OXOO
17	OOOO	OOOO	OXOO	OOOO
18	OOOO	OOOO	OOOO	OOOO
19	OOOO	OOOO	OOOO	OOOO
20	OOOO	OOOX	OOOO	OOOO
21	OOOO	OOOO	OXOO	XOOO
22	OOOO	OOOO	OOOO	OOOO
23	XOXO	OOOO	OOOO	OOOO
24	OOOO	OOOX	OOOO	OOOO
25	OOXO	OOOO	OOOO	OOXO
26	OOOO	OOOO	OOOX	OOOO
27	OOOO	OOOO	OXOO	OOOO
28	XXOO	OOOO	OOOO	OOOO
29	OOXO	OOOO	OOOO	OOXO
30	OOOO	OOOO	OOOX	OOOO
31	OOOO	OOOO	OXOO	OOOO
32	OXOO	OOOO	OOOO	OOOO
33	OOOO	OOOO	OOOO	XOOO
34	XOOO	XXOO	OXOO	OOOO
35	OOOO	OOOO	OOOO	OOOO
36	OOOO	OOOO	OOOO	OOOO
37	OOOO	OOOO	OOOO	XOOO
38	OOOO	OOOO	OXOO	OOOO
39	OOOO	OOOO	OOOO	OOOO
40	OOOO	OOOO	OOOO	OOOO
41	OOOO	OOOO	OOOO	OOOO
42	OOOO	OXOO	OOOO	OXOO
43	OXOO	OOOO	OOOO	OOOO
44	OOOX	OOOO	OXOO	OOOO
45	OOOO	OOOO	OOOO	OOOO
46	XOOO	OXOO	OOOO	OXOO
47	OXOO	OOOO	OOOO	OOOO
48	OOOX	OOOO	OXOO	OOOO
49	OOOO	OOOO	OOOO	OOOO
50	XOOO	OOXO	OXOO	OOOO
51	XOOO	OOOO	OOXO	OOOO
52	XOOO	OOOO	XOOO	OOOO
53	XOOO	OOOO	OOOO	OOOO
54	XXOO	OOXO	OOOO	OOOO
55	XOOO	OOOO	OOXO	OOOO
56	XOOO	OOOO	XOOO	OOOO
57	OOOO	OOOO	OOOO	OOOO
58	OOOO	OOOO	OXOO	OOOO
59	XOOO	OOOO	OOOO	OOOO
60	XOXO	OOOO	XOOO	OOOO
61	XOOO	OOOO	OOOO	OOOO
62	XOOO	OOOO	OXOO	OOOO
63	XOOO	OOOO	OOOO	OOOO
64	XOXO	OOXO	XOOO	OOOO

Fig.4 Error bit map measured on the 1-kbit RAM chip.