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Clean Silicon Wafer Surface by a Slight Etch Method

Ritsuo Takizawa, Toshiro Nakanishi, Kouichirou Honda, and Akira Ohsawa

FUJITSU Laboratories LTD.

1015, Kamikodanaka, Nakahara-ku, Kawasaki 211, JAPAN

We have developed a new cleaning method called the slight etch (**SE**) which dissolves the silicon wafer surface using an HNO_3-HF based solution with an extremely low HF concentration. The removal of 30 nm in depth by SE reduces the Fe surface concentration by one tenth in comparison with conventional RCA method and all measured elements are reduced to below a concentration of 10^{10} cm^{-2}, without surface degradation in roughness. The significantly improved C-t retention time and defect density of SiO_2 are also confirmed. We propose that this new method as a useful substitute for RCA.

1. Introduction

Residual trace impurities such as heavy and alkaline metals, particles, and hydrocarbons on silicon wafer surfaces can have detrimental effect on the electric characteristics, reliability, and production yield of devices, especially sensitive MOS VLSIs. Hence, completely clean silicon surfaces are intensely required for VLSI development.

Silicon wafers prior to device fabrication are generally cleaned with the RCA method proposed by Kern[1] and/or a modified method. However, it is not easy to reduce surface heavy metals, such as Fe, below a concentration of 10^{11} cm^{-2} [2]. Some reports have been made concerning the behavior of heavy metals on the silicon wafer surfaces in the cleaning solution. Harmful Fe impurities were introduced to the silicon native oxide, forming an Fe(III)-O complex[2] in an oxidizing agent, such as the HNO_3 solution. Cu impurities, however, adhered to the surface reacting directly with the silicon[3] in a reducing agent, such as a HF solution.

Based on this contamination mechanism, we developed a new cleaning method called the slight etch (**SE**) method which slightly dissolves the silicon surface using a HNO_3-HF based solution. Although HNO_3-HF based systems are well known to dissolve silicon[4], using an extremely low HF concentration resulted in ultraclean silicon surfaces without a degradation in roughness. We propose SE as a useful substitute for the RCA method.

2. Experiments

Boron-doped 10 ohm-cm (100) Czochralski-grown silicon wafers, 100 mm in diameter, were used in our experiments. All wafers were first cleaned with the conventional RCA method (NH_4OH/H_2O_2-HF-HCl/H_2O_2-NH_4OH/H_2O_2), then some wafers were immersed into a temperature-controlled solution containing HNO_3 (60%) and HF (<0.1%). After immersion, the wafers were rinsed with deionized water for 10 minutes, and dried using a quartz heater.

The surface roughness before and after the SE was characterized using a Mirau optical profilometer[5] (**TOPO-2D;** Wyko Corp.) and reflection electron microscopy[6), 7] (REM). The concentration of surface metals was determined by the atomic absorption spectrophotometry with HF vapor phase decomposition[8] of the native oxide formed by the cleaning, and a 20-nm-thick thermal oxide formed at 1000°C after cleaning. Aluminum electrodes were formed on the thermal oxide to measure the C-t retention time at 50°C and the defect density of the oxide.

3. Results and Discussion

The etch rate of the silicon surface by the SE was estimated from the change in weight before and after cleaning, assuming uniform etching. The detection limit of the etch depth is about 3 nm for a 100-mm wafer. The etch rate increases with the HF concentration. The etch depth can be controlled as far as 300 nm by adjusting both the HF concentration and immersion time. This cleaning process produces stable native oxide (about 1 nm thick) on silicon surfaces, because etch reaction rate is thought to be determined by the dissolution rate of the oxide in the extremely low HF concentration. The etch selectivity of silicon by the SE is also measured to be about 10 with respect to the thermal SiO_2 layer. This method is effective for purifying thermal oxide patterned wafers.

The Mirau optical profilometer[5] consists of a conventional, reflection-type optical microscope with a Mirau two-beam interferometer attachment. Since the interference patterns of the surface (observed area: 0.5 μm x 665 μm) can be detected with a solid-state linear array of 1024 detector elements, one detector can measure roughness on the average of a 0.5 μm x 0.65 μm area on the silicon surface. The profilometer can thus reveal surface roughness of about 5-500 μm in period. Fig. 1 graphs the correlation between the Rrms determined by the profilometer and the etch depth. Rrms is defined by the root mean square of the height distribution across the silicon measured at 1024 points. The error bars show the standard deviation for several measurement at different points on the wafer. Since Rrms does not depend on etch depth to 300 nm, the surface roughness of 5-500 um in period is confirmed not to be degraded by the SE.

Reflection electron microscopy (REM) images are known to be able to reveal the surface roughness of about 20-5000 μm in period[6), 7]. The dependence of surface roughness calculated from REM images on the etch depth is shown in Table 1. It is evident that the roughness after 30 nm of etching is about the same as that of after only RCA, 1-2 nm in height and 50-500 nm in period. Etching

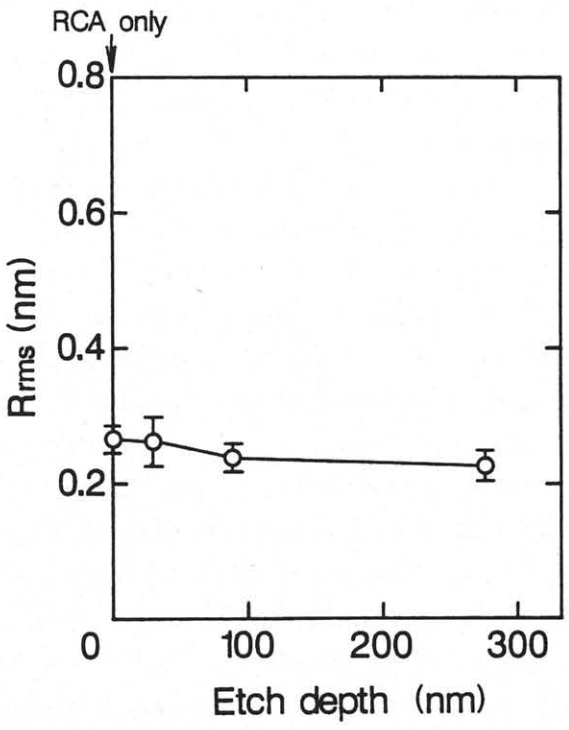

Fig.1. Correlation between Rrms measured by Mirau optical profilometer and etch depth.

Table 1 Dependence of surface roughness revealed by REM on etch depth.

Etch depth (nm)	REM image	Surface roughness (nm)	
		Height	Period
0 (RCA only)		1–2	50–100
30		1–2.5	50–100
270		2–5	50–100

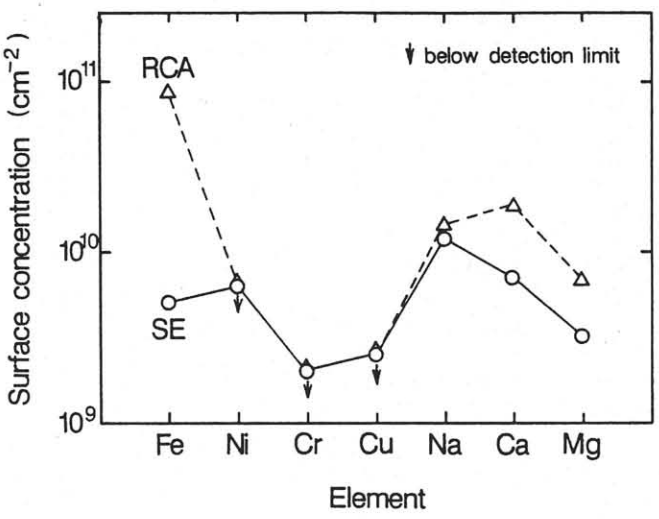

Fig. 2 Difference of surface impurities just after cleaning between the SE and RCA.

of 270 nm, however, degrades the surface roughness with respect to height.

The difference in surface metal impurities without oxidation before and after the SE (etch depth: 30 nm) following RCA is shown in Fig. 2. It is evident that the SE reduces surface Fe concentration by a factor of ten and Ca and Mg by a third when compared to RCA only. The removal of 30 nm in depth reduces all measured elements below concentrations of 10^{10} cm^{-2}. This is due to the removal of the shallow contaminated region, which is thought to be introduced on the silicon wafer surface during polishing process.

Fig. 3 shows the dependence of surface impurities after oxidation on the etch depth. This oxidation was performed at the same time as that of Al-gate MOS device fabrication. The surface concentration level is slightly higher than the result without oxidation shown in Fig. 2. This is because the concentration in Fig. 3 includes the contamination introduced during oxidation process. Though removal of 30 nm reduces the surface metal concentration as shown in Fig. 2, etching beyond 30 nm gives no further improvement.

The dependence of the C-t retention time at 50°C and defect density of SiO_2 on the etch depth is graphed in Fig. 4. The defect density is obtained from the dependence of the yield (breakdown field > 8 MV/cm) on the gate area (0.25 and 0.09 cm^2). The breakdown strength is defined as the voltage required to give a leakage current of 50 μA. This figure demonstrates that the removal of 30 nm improves retention time by a factor of 2 and the defect density by one third. This improvement is due to the removal of impurities from the silicon surface without a degradation in roughness. Etching beyond 30 nm in depth gives no further improvement and increases the deviation, especially in defect density. This degradation is caused by an increase in surface roughness.

4. Conclusion

We developed the slight etch method which dissolves the silicon wafer surface using an HNO_3-HF based solution with an extremely low HF concentration. The etch rate

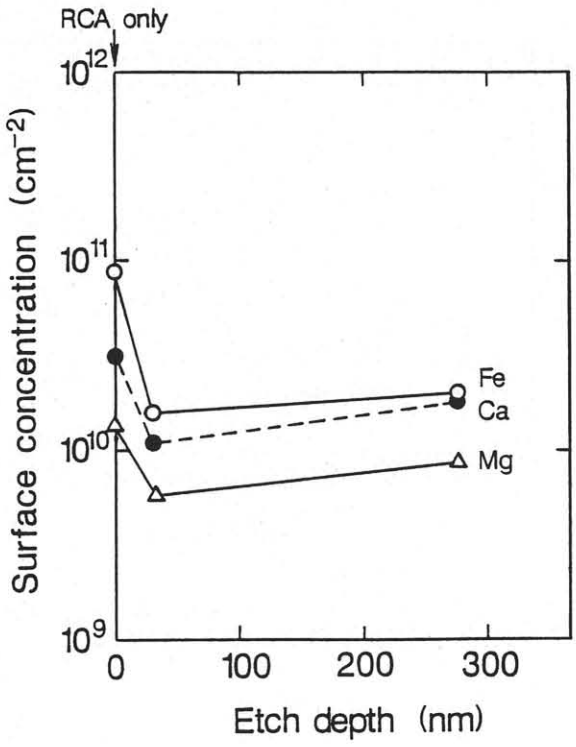

Fig. 3 Dependence of surface impurities after oxidation on etch depth.

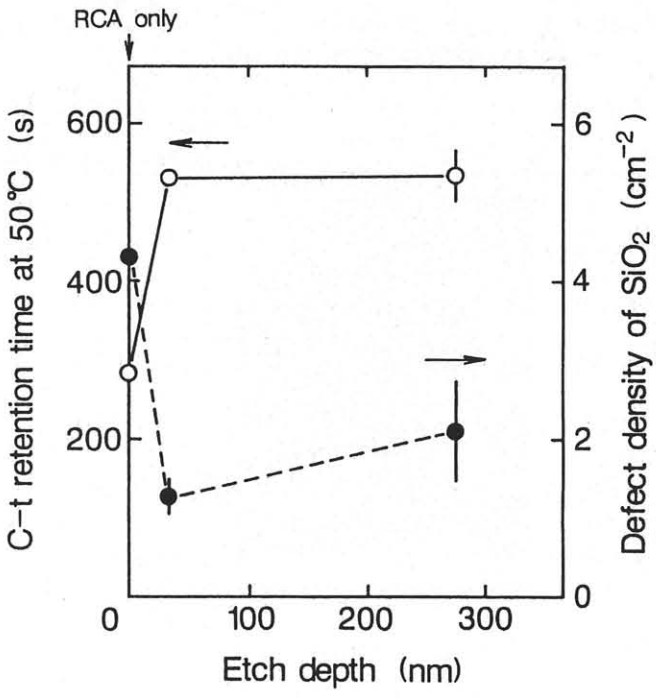

Fig. 4 Improvement of MOS device characteristics by the SE.

can be controlled to 300 nm by adjusting the HF concentration and immersion time. The removal of 30 nm in depth reduces surface Fe concentration by a factor of ten and Ca and Mg by a third when compared to conventional RCA, without surface degradation in roughness. The significantly improved C-t retention time and SiO_2 defect density due to the SE is also confirmed. Since the etch selectivity of silicon for thermal SiO_2 is about 10, this method is also ideal for purifying thermal oxide patterned wafers. The SE method can be practically applied to fabrication processes for high-performance devices as a substitute for conventional RCA.

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References

1) W. Kern and D. A. Puotinen: RCA Review 31 (1970) 187.
2) R. Takizawa, T. Nakanishi, and A. Ohsawa: J. Appl. Phys. 62 (1987) 4933.
3) Y. Okui, T. Honda, T. Ogawa, N. Niwayama, M. Yoshida, and K. Wada: 47th Fall Meeting of the Japan Soc. of Appl. Phys. (1986)155 (in Japanese).
4) B. Schwartz and H. Robbins: J. Electrochem. Soc. 123 (1976) 1903.
5) B. Bhushan, J. C. Wyant, and C. L. Koliopoulos: Appl. Opt. 24 (1985) 1489.
6) K. Honda, A. Ohsawa, and N. Toyokura: Appl. Phys. Lett. 48 (1986) 779.
7) K. Honda, R. Takizawa, and A. Ohsawa: J. Appl. Phys. 63 (1988) 2637.
8) A. Shimazaki, H. Hiratsuka, Y. Matsushita, and S.Yoshii: Ext. Abst. of 16th Conf. on Solid State Devices and Materials (Kobe, 1984) p. 281.