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Integration of GaAs SISFET and GaAs Inversion-Base Bipolar Transistor

Kazuhiko Matsumoto, Yutaka Hayashi, Takeshi Kojima,
Toshiyuki Nagata, Tomomi Yoshimoto
Electrotechnical Laboratory MITI
Tsukuba-shi, Ibaraki, 305, JAPAN

Abstract: The first integration of a GaAs FET type device and a GaAs bipolar transistor type device was achieved using the GaAs SISFET and GaAs Inversion-base Bipolar Transistor (GaAs IBT). The GaAs SISFET showed the transconductance of g_m=123mS/mm and the GaAs IBT showed the current gain of β=5 for the common emitter configuration at 77K.

1. Introduction

In order to get a small access time in a GaAs large-scale integrated circuit, it is one of the best solution to integrate a GaAs FET with a feature of a low power consumption and a GaAs bipolar transistor with a feature of a high current drivability. However, the structures of a conventional GaAs FET (HEMT or MESFET) and a GaAs bipolar transistor (GaAs HBT) are quite different to each other. So, it is difficult to integrate them on the same wafer. While the GaAs SISFET and the GaAs Inversion-Base Bipolar Transistor (GaAs IBT) have similar device structures, it is much easier to integrate them on the same wafer. In the present paper, the first integration of a GaAs FET type device and a GaAs bipolar transistor type device using a

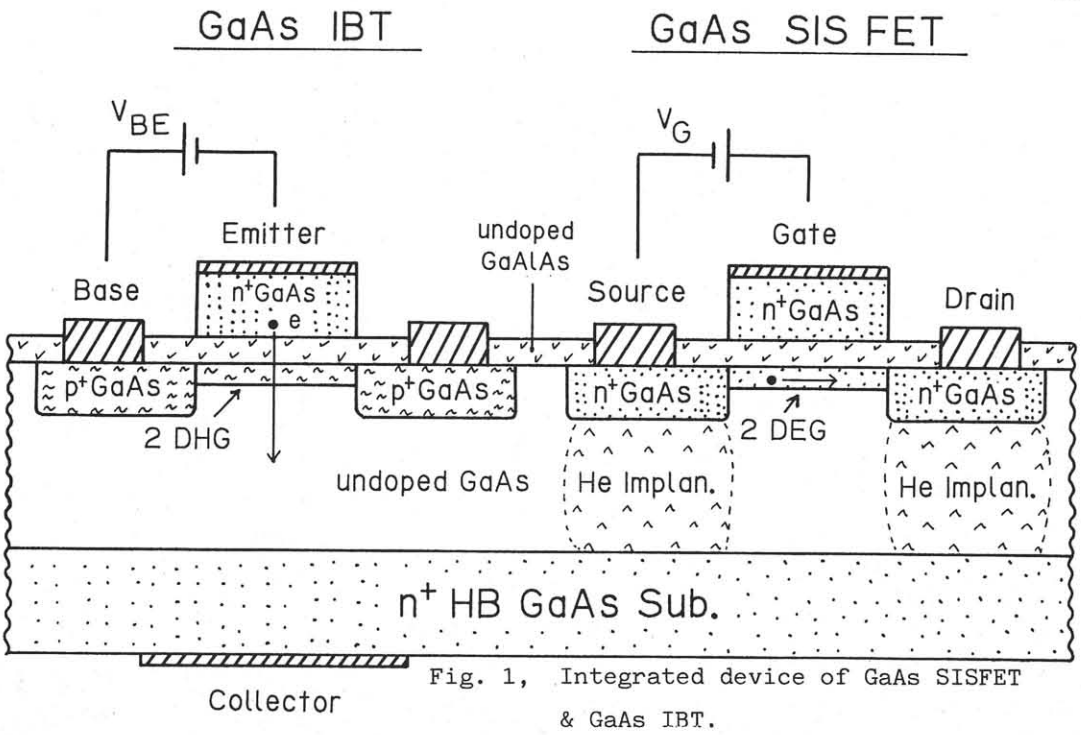

Fig. 1, Integrated device of GaAs SISFET & GaAs IBT.

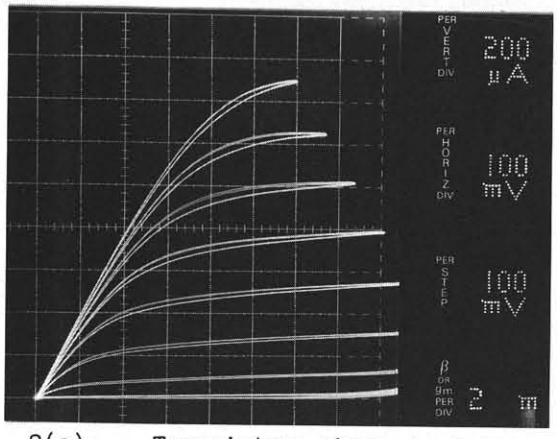

Fig. 2(a), Transistor characteristics of GaAs SISFET at 77K. Gate bias is applied from V_G=0V to 0.7V. Threshold voltage is V_{th}=88mV.

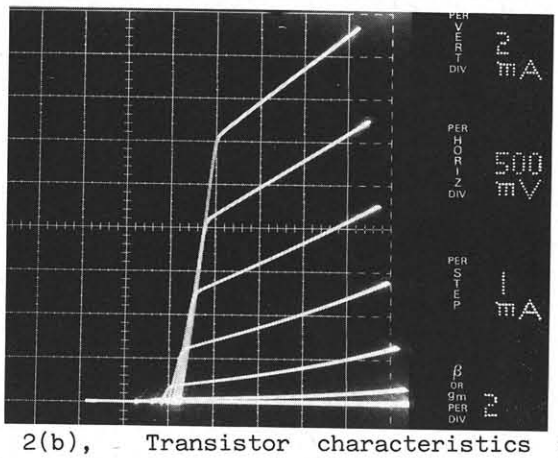

Fig. 2(b), Transistor characteristics of GaAs IBT at 77K. Base current is aplied from 0mA to 6mA.

GaAs SISFET and a GaAs IBT will be presented.

2. Experiment

2-1. Structure & Characteristics

Figure 1 shows the schematic structure of the integrated device of the GaAs SISFET and the GaAs IBT. By applying the positive bias to the gate of the GaAs SISFET, two dimensional electron gas is induced at the undoped GaAlAs/undoped GaAs interface, which works as a channel of the FET. Thus, the GaAs SISFET works as a FET-type transistor. Under the source and drain n^+ regions, there are herium implanted regions which isolate the source and drain from the n^+ GaAs substrate.

By applying the negative bias to the emitter of the GaAs IBT, a two dimensional hole gas is induced at the undoped GaAlAs/undoped GaAs interface , which works as an extremely thin base. The electrons in the emitter go over the emitter barrier, pass through the two dimensional hole gas base, and reach the collector. Thus, the GaAs IBT works as a bipolar-type transistor.

The GaAs SISFET and IBT have the similar device structures as shown in Fig. 1. The structural difference between them is conduction types of electrodes which are formed by an ion implantation: the source and drain for the SISFET and the external base for the GaAs IBT.

The crystal for the devices is grown by MBE on the n^+GaAs substrate, i.e., an undoped GaAs (1μm) / an undoped $Ga_{0.6}Al_{0.4}As$ (300Å) and an undoped graded $Ga_{1-x}Al_xAs$ ($x=0.4 \rightarrow 0$) / an n^+GaAs ($n=3\times10^{18}/cm^3$, 5000Å). The gate length and the width of the GaAs SISFET are Lg=2μm and Wg=20μm. The emitter size of the GaAs IBT is $50\times50\mu m^2$. For the source and drain n^+ regions and the external base p^+ region, the silicon ions (90keV, $1\times10^{13}/cm^2$: 100keV, $2\times10^{13}/cm^2$: 190keV, $4\times10^{13}/cm^2$) and magnesium ions (90keV, $5\times10^{13}/cm^2$: 150keV, $8\times10^{14}/cm^2$) were implanted, respectively. After the annealing process of 800°C for 100seconds, herium ions (120keV, $1\times10^{12}/cm^2$) were implanted through the source and drain n^+GaAs regions.

Figure 2(a) shows the transistor characteristics of the GaAs SISFET at 77K. The positive gate bias from V_G=0V to V_G=0.7V with 0.1V step was applied. The gate bias of up to V_G=+1.4V could be applied with no gate leak current. The transconductance, the drain conductance, and the threshold voltage are g_m=123mS/mm, g_D=3.3mS/mm at V_G=0.6V, V_D=0.6V, and V_{TH}=+88mV, respectively. The source resistance is R=130ohm, which is

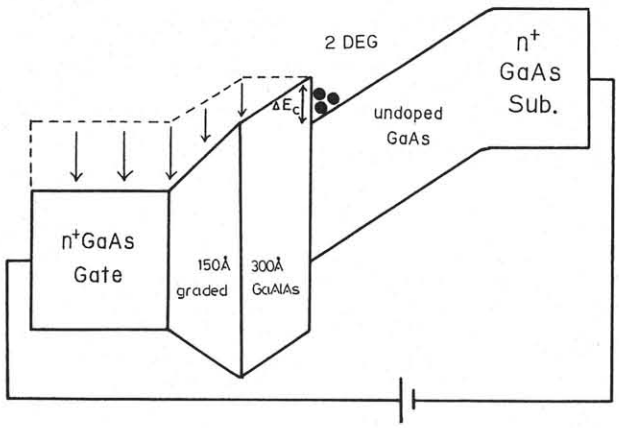

Fig. 3(a), Energy diagram for SISFET operation mode. Positive bias is applied to the n^+GaAs gate.

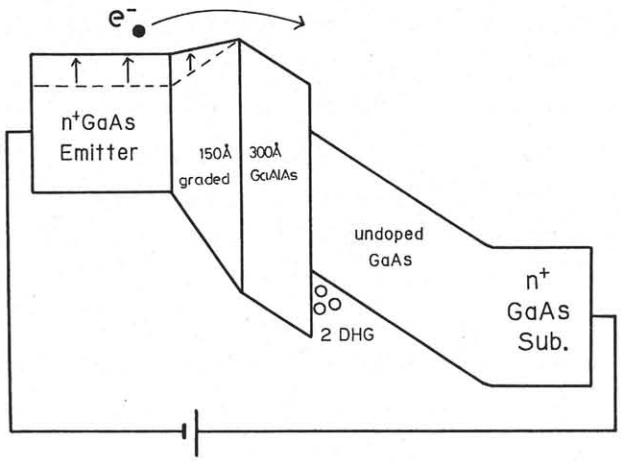

Fig. 3(b), Energy diagram for IBT operation mode. Negative bias is applied to the n^+GaAs emitter.

slightly higher than that of a typical self-aligned GaAs FET. The high source resistance is attributable to the high sheet resistance and a high contact resistance of the source n^+GaAs region of Rs=600 Ω/□ and Rc=0.7 Ω mm, respectively, which are deteriorated by the herium implantation.

Figure 2(b) shows the transistor characteristics of the GaAs IBT at 77K for the common emitter configuration. The current gain of β =5 was obtained. The output conductance was fairly large value of g_{out}=3.2mS. The offset voltage at which the collector current begins to flow is V_{offset}=0.9V.

In order to obtain these transistor characteristics, two major problems have been solved. These problems are discussed in the follwing sections. (2-2, 2-3)

2-2, Effects of the graded layer

For the GaAs SISFET, the electrons flowing in the channel must not go over the undoped GaAlAs barrier layer. While for the GaAs IBT, the electrons in the n^+GaAs emitter must go over the undoped GaAlAs barrier layer to reach the collector. In order to solve this discrepancy, we adopted the undoped "graded $Ga_{1-x}Al_xAs$ layer" at the side of the n^+GaAs/undoped GaAlAs interface. (See the crystal structure in 2-1.)

Figure 3(a)(b) show the energy band diagrams along the active region of the device, i.e., the n^+GaAs / undoped GaAlAs /undoped GaAs and n^+GaAs substrate. Figure 3(a) is the case of the SISFET-mode operation. In this case, the conduction band of the n^+GaAs layer goes downward from the zero biased condition (dashed line.) However, the energy gap ΔEc between the undoped GaAlAs barrier layer and the undoped GaAs channel layer is not modulated by the applied bias. Therefore, the induced electrons are confined at this interface.

Figure 3(b) is the case of the IBT-mode operation. In this case, the conduction band of the n^+GaAs layer goes upward, and the conduction band of the graded layer becomes flat. As a results, the energy barrier ΔEc between the n^+GaAs layer and the undoped GaAlAs layer is lowered by the applied bias, which effect enhances the electron injection from the n^+GaAs emitter to the undoped collector.

Consequently, the GaAlAs layer with the graded composition layer enhances the electron injection from the emitter to the collector for the GaAs IBT, and confines the

electrons in the channel for the GaAs SISFET.

2-3, Isolation by He Implantation

The source and drain n^+GaAs regions of the GaAs SISFET shown in Fig. 1 must be electrically isolated from the n^+GaAs substrate in order to eliminate the leak drain current through the substrate. For this purpose, herium (He) ions were implanted through the source and drain n^+GaAs regions to make the insulated layer under there. However, the high dose of the implanted herium ion deteriorate the sheet resistance of the source and drain n^+GaAs. Therefore, the optimum amount of the dose of the herium ion must be selected. The parameters used in the present experiments are listed in the inset of Fig. 4. The degree of the isolation was confirmed by measuring the current i between the drain n^+GaAs region and the n^+GaAs substrate at the applied bias of 1V as shown in the inset of Fig. 4. Figure 4 shows the dependence of the current i on the dose of the implanted herium ions. The current i decreases more than three orders of magnitude when the herium dose exceeds $7\times10^{11}/cm^2$. The leak current density must be lower than $1A/cm^2$ to suppress the drain leak two orders of magnitude less than the drain current. On the same time, the sheet resistance Rs of the n^+ implanted region must be low enough. Upon these consideration, the implantation condition of He ions was determined to be $1\times10^{12}/cm^2$, 120keV, and that of silicon ions for the n^+GaAs region was determined as listed in #3. Under these implantation conditions, the sheet resistance of Rs=600 ohm/□ was obtained with the sufficient isolation to the substrate.

3. Conclusion

We have succeeded in integrating the GaAs FET and bipolar transistor on the same wafer. Further improvement of the characteristics of the SISFET and IBT will be expected by the optimization of the condition of the ion implantation, the structure of the emitter barrier, etc.

	t	Si implan.	anneal	He
#1 ○	1um	70keV : $1\times10^{13}cm^2$ 100keV : $2\times10^{13}cm^2$	800C 30sec.	70keV
#2 ●	0.5nm	70keV : $1\times10^{13}cm^2$ 100keV : $2\times10^{13}cm^2$	800C 30sec.	70keV
#3 Δ	1um	70keV : $1\times10^{13}cm^2$ 100keV : $2\times10^{13}cm^2$ 190keV : $4\times10^{13}cm^2$	800C 100sec.	120keV

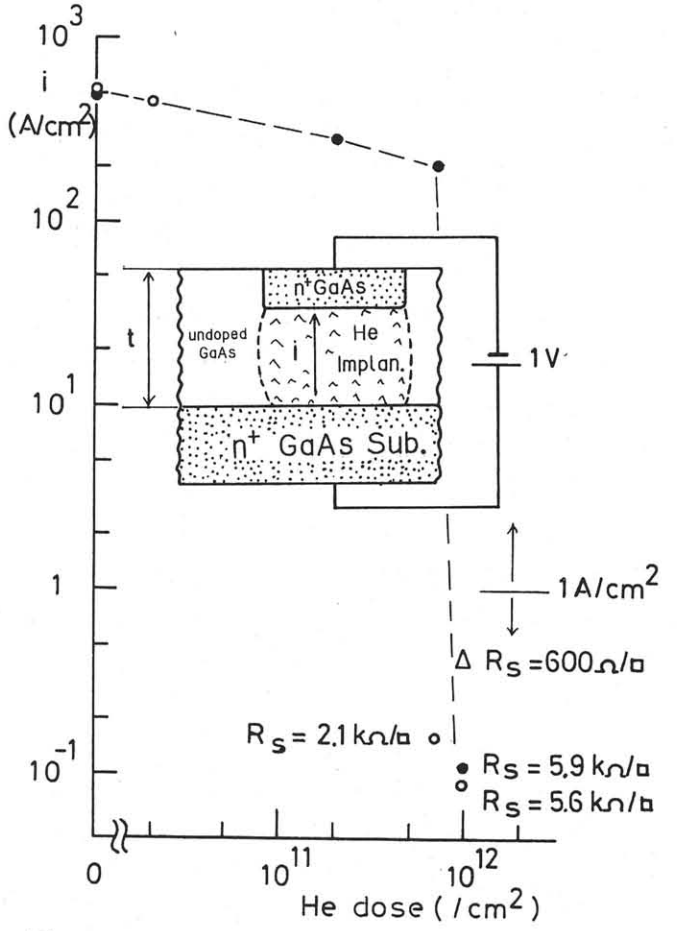

Fig. 4, Dependence of leak current on implanted He dose.