Extended Abstracts of the 20th (1988 International) Conference on Solid State Devices and Materials, Tokyo, 1988, pp. 549-552

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Down-Flow Process in VLSI Manufacturing

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The down-flow reactor in which the wafers are located far from the complex plasma environment is a powerful tool in understanding the neutral chemistry in the plasma. In the course of pursuing the unknown chemistry, a novel down-flow process which is very useful for the VLSI manufacturing has been invented. In aspects of practical use, the down-flow process has the great advantage of damageless processing, and therefore, will be increasingly needed to produce ULSI devices in future.

1. Introduction

In the past ten years, dry etching technologies employing a low temperature plasma have been rapidly introduced into the VLSI production line, because the wet chemical etching processes do not allow fine line engraving to be reproducibly obtained. Especially, a reactive ion etching (RIE)[1], which utilizes energetic ion bombardment, realized the directional etching feature, and strongly promoted the shrinkage of minimum device feature size. The charged particle bombardment, however, involves the generation of serious radiation damage such as gate oxide breakdown[2].

As another extreme of dry etching technologies, the down-flow etching[3], whose process is carried out using neutral species alone, has been used in VLSI manufacturing. Since the etching feature is usually isotropic, down-flow etching is not applicable to engraving finer patterns. The process, however, is much milder than RIE, which makes it possible to etch various materials without any radiative damage. Because of this great advantage, down-flow etching attracts notice again in VLSI manufacturing, and its concept is now being expanded into other wafer processings[4~7].

This paper reports recent progress in the down-flow process, and refers to the future trend.

2. Down-flow reactor

Figure 1 shows a layout diagram for down-flow reactor, whose design is called a chemical dry etching system[8]. The reaction chamber is located far from the 2.45 GHz microwave discharge tube. The wafers are chemically etched by transported long lived species such as fluorine atoms.

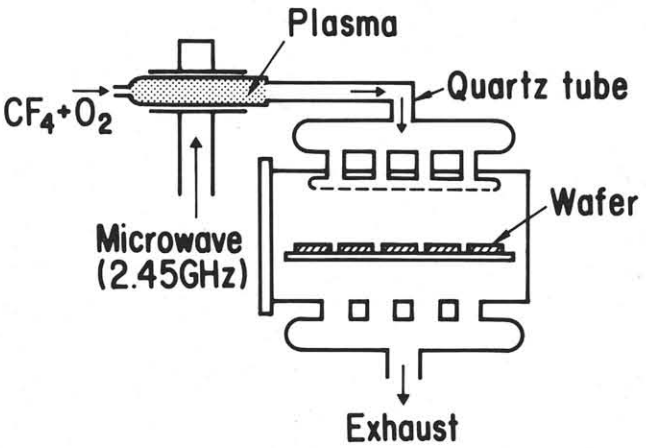

Fig. 1 Layout diagram of down-flow reactor.

Since the charged particle bombardment and the UV light irradiation are completely eliminated from the reaction chamber, the wafers do not suffer any radiative damage. Furthermore, the configuration in Fig. 1 offers a very efficient tool for investigating the reaction mechanism for a solid with neutral species, because the wafers are set out of the complex plasma environment. All of the following applications were produced in the course of studying what happens in the gas phase or solid surface.

3. Recent progress attained in the down flow process

3.1 Highly selective Si_3N_4 removal on thin SiO_2 film

Si_3N_4 is widely used as a mask material for local oxidation of silicon, LOCOS[9], in VLSI manufacturing. Since the pad SiO_2 film thickness becomes thin to minimize bird's beak length, Si_3N_4 has to be removed with high selectivity in regard to the underlying pad SiO_2 film. This requirement was achieved employing the gas phase reaction between fluorine and chlorine atoms.

Figure 2 shows Si_3N_4 and SiO_2 etch rates as a function of Cl_2 flow rate[4], where NF_3 flow rate was kept at 30 sccm. SiO_2 etch rate decreases monotonically with increasing Cl_2 flow rate, and becomes zero at 60 sccm Cl_2 flow rate. On the other hand, Si_3N_4 etch rate maintains a finite value even in the high Cl_2 concentration region. As a result, the etch rate ratio for Si_3N_4 to SiO_2 becomes infinite. By adding a lot of Cl_2 to NF_3, most fluorine atoms are rapidly converted to interhalogen molecules, FCl, by titration reaction with Cl_2 in the gas phase[10]. The resultant FCl etches Si_3N_4, whose chemical bond property is rather close to that for Si, while FCl does not react with SiO_2 without any radiative irradiations[11].

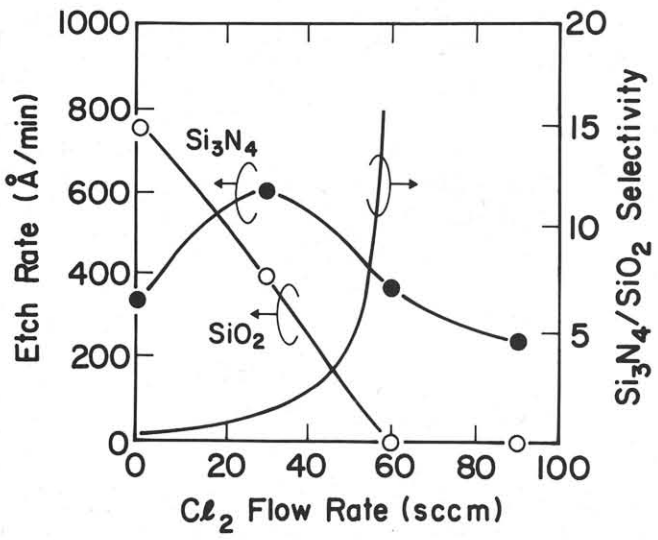

Fig. 2 Si_3N_4 and SiO_2 etch rates vs. Cl_2 flow rate at 30 sccm NF_3.

Figure 3 shows results actually applied to Si_3N_4 removal on the thin pad SiO_2 film. Figures 3(a) and (b) show cross sectional views of LOCOS structure after Si_3N_4 removal. Under relatively low selectivity conditions, the chemically weakened portion of SiO_2 at the bird's beak corner was etched first by fluorine atoms, which cause the underlying Si substrate erosion (shown by an arrow in Fig 3(a)). On the other hand, the infinite selectivity allows Si_3N_4 removal with no Si substrate damage (Fig 3(b)).

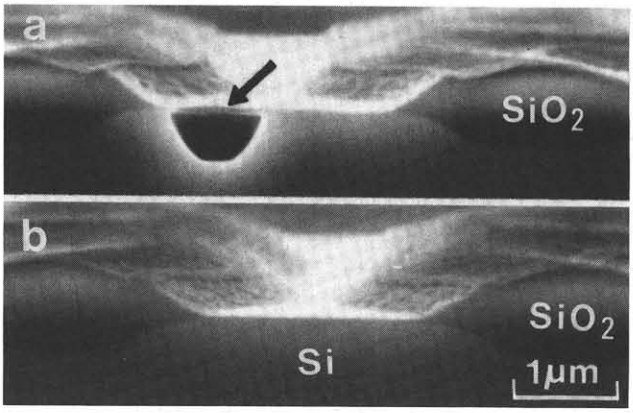

Fig. 3 Si_3N_4 removal in LOCOS. Si_3N_4/SiO_2 selectivities are (a) 10 and (b) infinite, respectively.

3.2 Resist-residue free ashing

An O_2 plasma ashing technique employing a barrel reactor is now used to strip the photoresist after RIE and ion implantation. However, the problem of persistent resist-residue in the VLSI production line is often encountered. Once such a resist-residue remained, it cannot be completely removed, no matter how long ashing is done. This persistent resist-residue problem was solved by the use of reaction of fluorine atoms with water vapor[5].

The origin of resist-residue is considered to be as follows. During the reaction of resist surface with oxygen atoms, the inner part of the resist is being baked by the heat of reaction[12]. As a result, crosslink reactions such as ester formation or oxidation of novolac resins in the posi-type photoresist take place to produce giant molecules. These crosslinked molecules exhibit strong resistivity for the attack of oxygen atoms, and remain as persistent resist-residue to the last (shown by an arrow in Fig 4(a)).

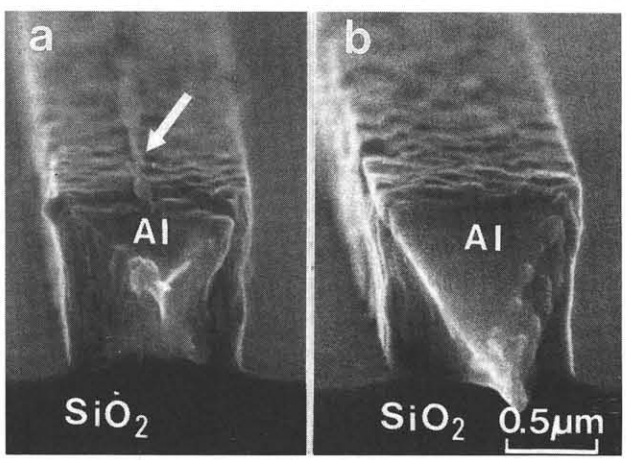

Fig. 4 Resist ashing after Al RIE. The ashing was implemented by the use of (a) O_2 plasma and (b) reaction between fluorine atoms and water vapor, respectively.

Water vapor was introduced into the reaction chamber to remove native oxide with hydrogen fluoride, which was produced by the following rapid reaction.

$$2F + H_2O \longrightarrow 2HF + O$$

However, against expectation, SiO_2 was not etched at all, and it was found that the resist after Al RIE was etched perfectly at high rate (Fig. 4(b)). In the present ashing technique, fluorine atoms react with resist polymer to extract hydrogen atoms. As a result, the weakened resist polymer is etched off effectively by a lot of oxygen atoms.

3.3 Smoothing roughened surface

Figure 5 shows Si etch rate as a function of O_2 to CF_4 flow rate ratio[6]. The Si etching with fluorine atoms is clearly suppressed by a large amount of O_2 addition. In the high O_2 concentration region, the etching products are oxidized in the gas phase to form low volatile oxyfluoride. The resultant oxyfluoride is redeposited on the Si surface, and limits the etching reaction of Si with fluorine atoms.

Generally, the equilibrium vapor pressure for gas phase species is low at a corner with negative curvature, as compared to that with a positive curvature[13]. Therefore, the oxyfluoride condensed preferentially at the dented plane on the roughened surface. Consequently, the etching proceeds quickly at a corner with positive curvature along with increasing time, which leads to smoothing a roughened surface. This idea is applied to smooth the roughened sidewall of a Si trench, and to round off the bottom corner with negative curvature (Fig. 6).

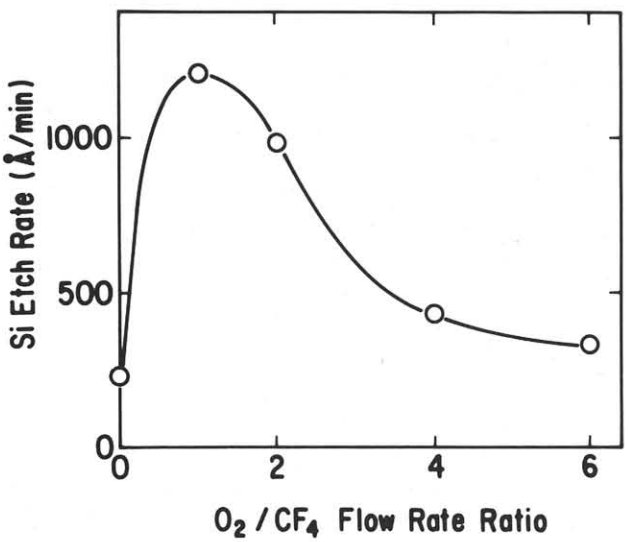

Fig. 5 Si etch rate vs. O_2 to CF_4 flow rate ratio.

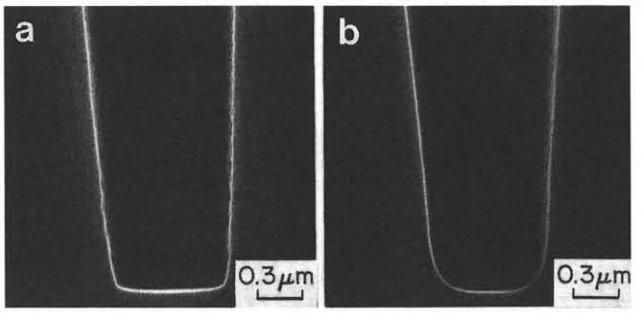

Fig. 6 Si trench features of (a) before and (b) after smoothing the roughened sidewall and rounding off the bottom corner with negative curvature, respectively.

3.4 Complete planarization for high aspect ratio grooves

As the minimum feature size for VLSI devices continue to decrease, high aspect ratio processes are required such as the Si trench capacitor and the multilayer metalization. Most of the film deposition techniques, however, cause overhang step coverage, which results in a void in the Si trench and a space between interconnection lines. These problems are not substantially prevented as long as the deposition was implemented by the use of gas phase species.

In order to investigate what kinds of species play important role in the CVD process, the authors separated the oxygen atom generation from the reaction

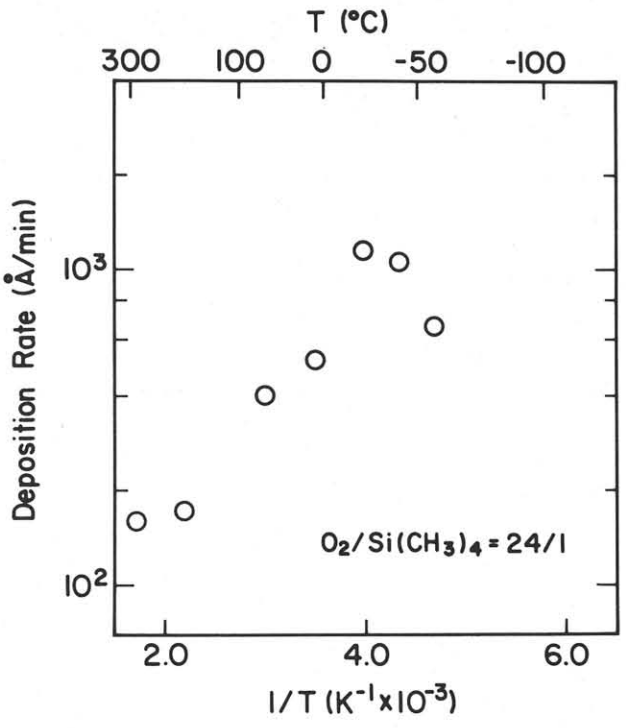

Fig. 7 Silicon oxide deposition rate vs. substrate temperature.

chamber. In the course of studying the deposition mechanism employing the reaction of oxygen atoms with $Si(CH_3)_4$, it was found that the deposition rate increases with decreasing substrate temperature(7), as shown in Fig 7 This result demonstrates that lowering substrate temperature enhances the adsorption rate for deposition species Based on this result, the substrate temperature was further reduced to the dew point of the adsorbates. As a result, the high aspect ratio Si trench was successfully filled, and completely planarlized with silicon oxide film, as if the liquid materials flow into the Si grooves just like water (Fig. 8).

In this method, partially oxidized species of $Si(CH_3)_4$, such as $(Si(CH_3)_3)_2O$, flow into the Si trench so as to minimize surface free energy, and is oxidized to change to a solid film from the bottom surface gradually. Therefore, the film properties are determined by the competitive reaction between liquefaction rate for the gas phase deposition species and oxidation rate for the liquefied materials. Actually, good quality film without a methyl group can be obtained by admitting the source gas intermittently, because the liquefied materials are sufficiently oxidized.

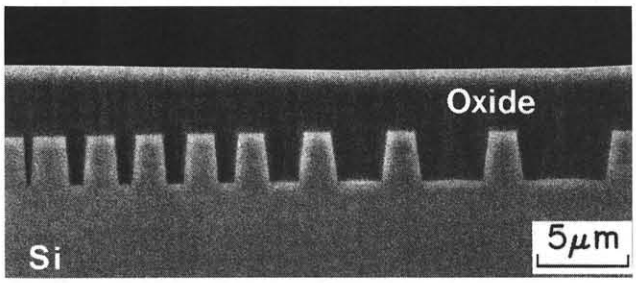

Fig. 8 Si trench feature after completely planarlized with silicon oxide film at −40°C.

4. Future trend for down-flow process

In the future ULSI manufacturing, the down-flow process with no radiative irradiation will be used as damage-free surface treatment such as cleaning, because clean and controlled surfaces are increasingly needed to produce ULSI devices. On the other hand, the energetic beam irradiation, whose energy is minimum where the beam-assisted chemical reaction occurs, enables realizing a directional process much milder than RIE(14).

However, beyond such aspects of practical use, the concept of separated system should be incorporated further in the field of plasma chemistry as a simplified research tool. A more precise understanding of complex phenomena in the plasma is the key to success in breaking the high wall in the nanometer field, and on reflection, inventing new applications of the down-flow process.

5. Conclusion

The down-flow process has been developed and actually applied to VLSI manufacturing. The wafers are fully separated from the plasma environment, which promises to build up damage free wafer processings such as cleaning, etching, deposition etc. The down-flow process employing neutral chemistry will continue to be a key technology in future, as well as an energetic beam-induced process such as RIE.

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