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Charge Losses of n-Doped Trench Cells

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N-doped trench cells exhibit increased charge losses when the cell plate voltage is reduced below 2.5V. This effect is attributed to tunneling of electrons from the valence band of the n-region into the conduction band thus contributing to the leakage current of the cell. Numerical simulations indicate that tunneling will occur preferently at the upper corners of the trench and imposes additional limitations to the doping concentrations and oxide thickness of this cell type.

1. Introduction

High cell capacitance and low leakage currents are the key features of a DRAM cell. In previous planar cells, generation currents in the space charge region and diffusion currents from the bulk have been considered the main leakage current sources. For n- doped trench cells with large junction area and small lateral dimensions punch through to the neighbouring trench often was regarded as the most important leakage current source. But due to high electric fields originating from thin oxides and high doping concentrations other leakage currents may dominate strongly depending on operation voltages.

For the n- doped trench cell used in the 4Mbit-DRAM [1] the origin of the charge losses of the cell and voltage range for safe operation has been evaluated.

2. Experimental details

The charge loss of the cell as a function of the applied voltage and temperature was measured with a test structure for refresh-time measurements shown schematically in Fig.1. The voltage of the bitline node 1 is

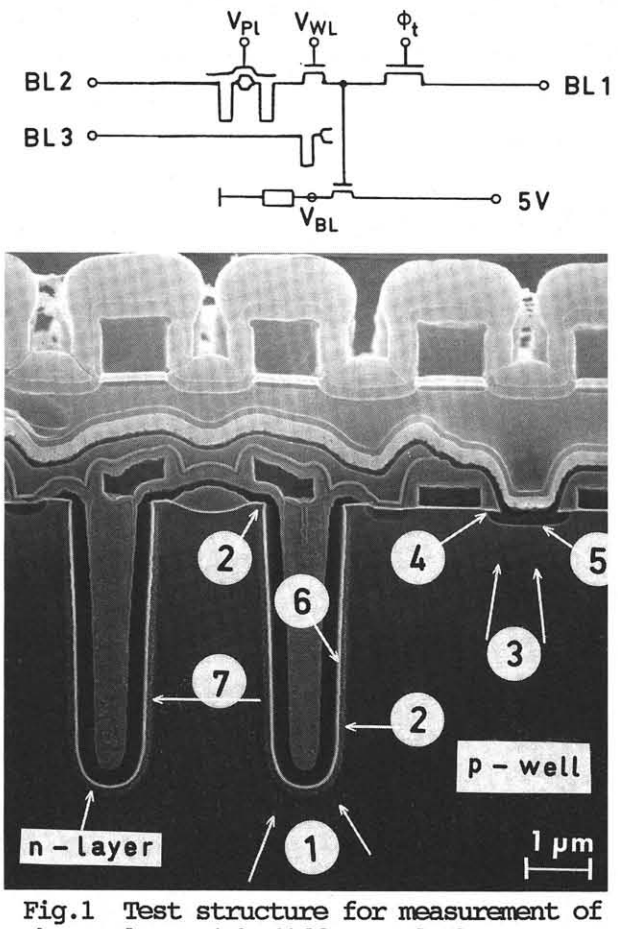

Fig.1 Test structure for measurement of charge loss with different leakage current contributions

sensed by a source follower circuit. After 50ms at 90°C (worst case condition), charge losses smaller than 5% typically are obtained using the nominal power supply voltage of 5V, a cell plate voltage of 2.5V and a substrate bias voltage of -2V. Changing the applied voltage may increase the charge loss up to 100%.

Different possible sources of the leakage current are also indicated in Fig.1. Label (3),(4),(5) refer to generation-, gated diode- and avalanche breakdown- current of the bitline node. Label (1),(2),(6),(7) refer to generation- , high electric field induced-, Fowler-Nordheim tunneling- and punch through- currents of the trench capacitor.

The cell under investigation has a trench depth of 5µm. Oxide thickness of the capacitor is 13nm, trench to trench distance is 1.8µm. The trench is embedded in a p-well with a doping concentration of 2E16cm^{-3} and surrounded by a n-layer (As,d=0.1µm) of (2-5)E18cm^{-3}.

3. Experimental results

3.1 Charge loss as function of voltage

The charge loss of the cell is influenced by the substrate bias voltage, the bitline voltage and by the cell plate voltage. Substrate bias voltage is mandatory to suppress punch through, parasitic transistor action at the surface and injection of electrons from the bitline nodes. The dominating leakage current depends on the cell plate voltage. In Fig.2 the remaining charge of the cell (after 50ms) is shown as a function of the cell plate voltage. For plate voltages greater than 2.5V and bitline voltages up to 8V charge losses of less than 5% are obtained. With decreasing cell plate voltage the charge loss increases strongly.

The leakage current at low cell plate

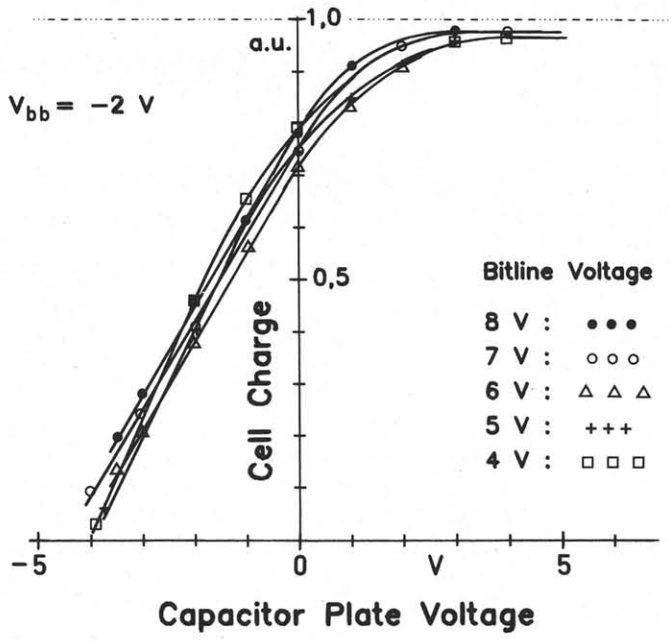

Fig.2 Cell charge as a function of cell plate voltage at different bitline voltages

voltages appears only in n- doped cells. Undoped trench cells do not exhibit this effect, as seen in Fig.3. Although only the n-layer seems to be responsible for this leakage mechanism, the onset of the current in the trench cell is observed at 1.5V lower voltages compared with a planar cell of the

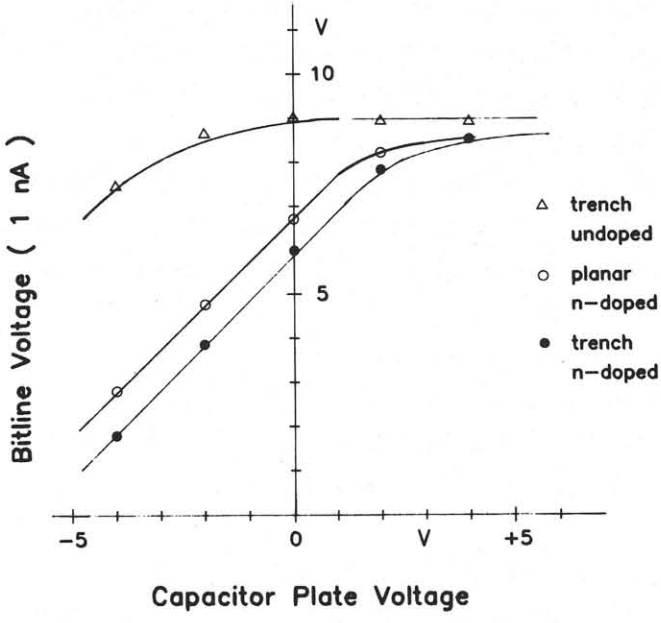

Fig.3 Bitline voltage at leakage current of 1nA/4k for different cell types

same doping concentration and oxide thickness.

3.2 Temperature dependence

In Fig.4 the temperature dependence of the leakage current contributions of the n-doped trench cell is shown. From the I-V characteristic as function of the bitline voltage, see insert of Fig.4, five dominating contributions can be separated according to the applied voltages. The current regions (1) and (3) of the cell and bitline node show an increasing current with temperature . From the activation energy of +0.6eV these are identified as generation currents at the pn-junctions. The maximum cell voltage is limited by avalanche breakdown of the bitline node to the substrate. It depends on substrate bias voltage and decreases with temperature (5). The most interesting intermediate current region (2), which depends on the cell plate

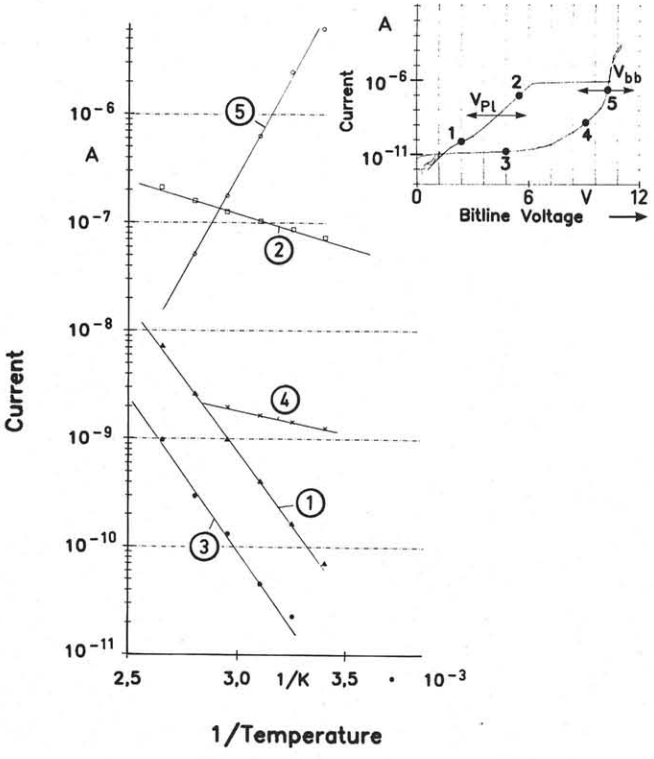

Fig.4 Temperature dependence of leakage currents. Labels refer to Fig.1

voltage, increases with temperature at an activation energy of +0.1eV. This value is typically for Zener tunneling and approximately the same value as reported for the Trench Transistor Cell [2]. In the n-doped trench cell electrons from the valence band of the highly doped n-region around the trench tunnel into the conduction band thus contributing to the leakage current.

The same activation energy was measured for the current region (4). Therefore tunneling seems to occur at the overlap of the bitline node to the transfer gate [3].

3.3 Simulations

Numerical simulations utilizing the 2D device simulator GALENE2 [4] have been carried out to investigate the different behaviour of the Zener tunneling in planar and trench type capacitors. We used a MOS-capacitor with n+ poly-Si gate and a gate oxide thickness of 13nm, which has a wide planar region and a sharp corner with a rounding radius of 10nm. The planar region and the corner is indicated in the insert of Fig.5 by the index p and c, respectively.

Under bias conditions, where the voltage drop in the gate oxide is more than 2.5V (Vbl=5V and Vpl<2.5V) the electrical field strength at the surface and the band bending reach the critical values for tunneling. Fig.5 shows the band bending at the interface as a function of the cell plate voltage Vpl for several As doping concentrations. At the trench corner c the band bending reaches the critical value Eg (band gap) at about 1.5V lower voltages compared with the planar region p. This agrees very well with the experimental results.

The doping concentrations which have to be used in the trench cell are in the critical range of (2-5)E18cm^{-3}. Lower doping concentrations would decrease cell

capacitance and higher doping concentrations would increase the width of the n-layer and punch through sensitivity.

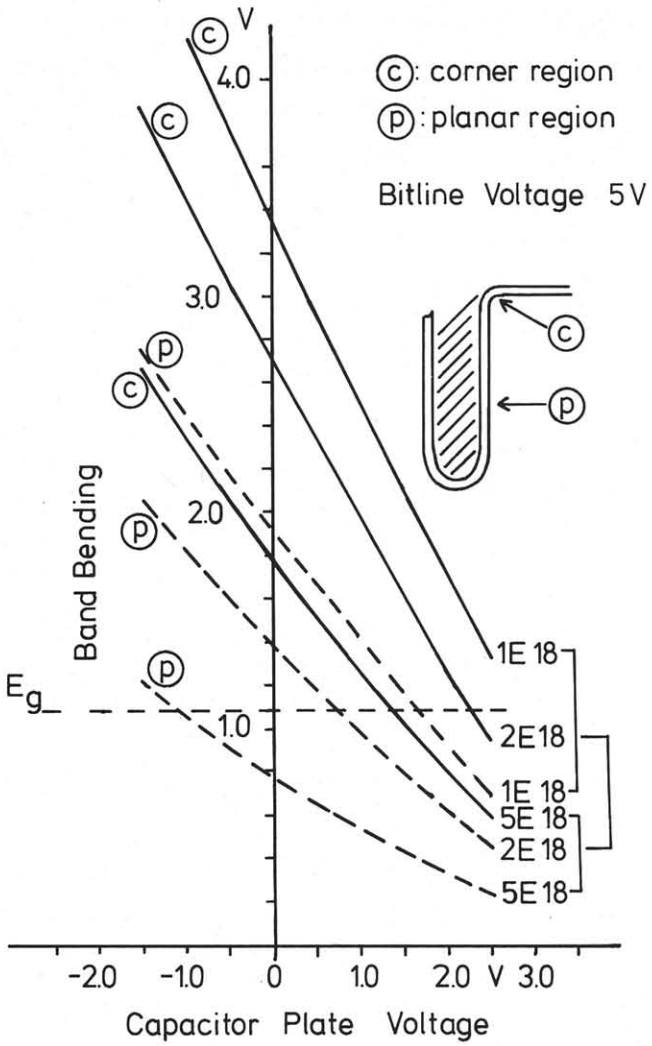

Fig.5 Band bending of n-region at planar and trench capacitors as a function of cell plate voltage for different doping concentrations

4. Conclusions

In the n-doped trench cell a new leakage current mechanism has been detected which dominates the charge loss of the cell at low cell plate voltages. From the activation energy of +0.1eV and from simulations a tunneling effect in the n-doped region occuring at the corners of the trenches is assumed. Using a cell plate voltage of 2.5 to 4V and substrate bias voltage the leakage currents can be kept below 0.5pA/cell, but oxide thickness, n- doping concentration and rounding of the trench corners have to be controlled properly. For 16M-cells with thinner dielectrics and doping concentrations of (1-5)E18cm^{-3} Zener tunneling must be taken into account in addition to the other leakage mechanisms.

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