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Device Degradation Due to Band-to-Band Tunneling

Hideyuki Matsuoka, Yasuo Igura and Eiji Takeda

Central Research Laboratory, Hitachi Ltd.

Kokubunji, Tokyo 185, Japan

A new device degradation due to band-to-band tunneling is investigated. In n-channel MOSFETs, holes created by band-to-band tunneling gain energy from the electric field in the drain region to surmount the Si-SiO_2 barrier and they are injected into the gate oxide. These trapped holes decrease the MOS threshold voltage and increase the transconductance, which is opposite to the degradation caused by the conventional 'hot' carrier effect. A simple model which explains this carrier injection is proposed. Experimental results are found to verify this model.

1. Introduction

In scaled MOSFETs with very thin oxide, the tunnel leakage current in gate-drain overlapped region creates serious problems and may become a limiting factor in MOS device miniaturization [1] [2] [3].

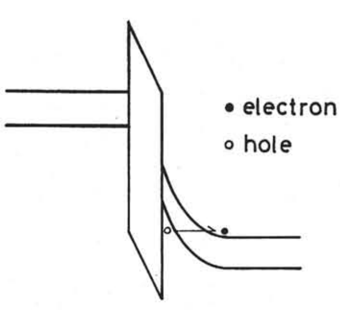

Fig. 1 Mechanism of band-to-band tunneling

Figure 1 shows the mechanism of band-to-band tunneling in the gate-drain overlapped region in n-channel MOSFETs. When the band bending is larger than the energy gap of Si, and the electric field at the Si-SiO_2 interface is strong enough, an electron can tunnel from the valence band to the conduction band, creating an electron-hole pair. The carriers created by band-to-band tunneling do not have enough energy to surmount the Si-SiO_2 barrier and have been thought not to affect the device characteristics. However, this study has proved this consideration to be insufficient and found that such carriers actually cause device degradation.

This paper studies such device degradation, particularly from the viewpoint of device reliability. Device degradation are discussed for both n- and p-channel MOSFETs with single drain structure. A new mode of device degradation is found, and a simple model which well explains the experimental results is proposed.

2. Experimental results in n-channel MOSFETs

The time dependence of the drain leakage current I_{ld} and the tunnel threshold voltage $V_{th}{}^{t}$ of n-channel MOSFET under two different stress conditions are shown in Fig. 2. Tunnel threshold voltage is defined as the drain voltage V_D at which I_{ld} is 0.01 pA/μm when $V_{SUB} = V_G = 0$ V. Figure 2 indicates the increase of $V_{th}{}^{t}$ and decrease of

I_{ld}, which implies the hole trapping in the gate oxide. This hole trapping increases the electric potential of the gate electrode and decreases the effective voltage difference between the drain and the gate.

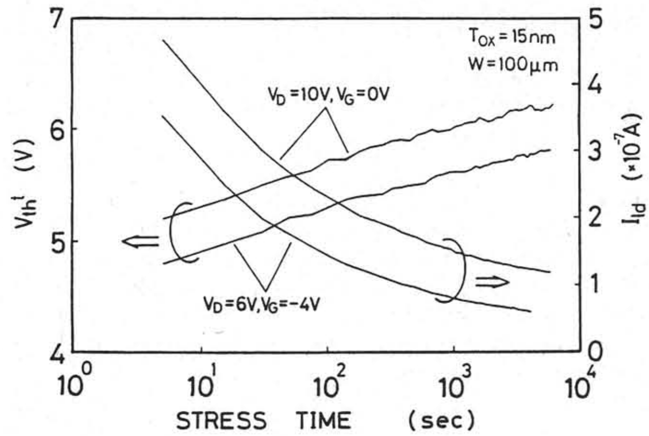

Fig. 2 Time dependence of I_{ld} and V_{th}^t in n-channel MOSFET

This hole trapping also affects the characteristics of MOS channel region. The time dependence of the shift of MOS threshold voltage ΔV_{th}^t and transconductance change $\Delta G_m/G_m$ are shown in Fig. 3. V_{th}^m decreases and G_m increases, which is expected from the hole trapping. This degradation is opposite to that caused by the 'hot' carrier effect previously reported [4] [5].

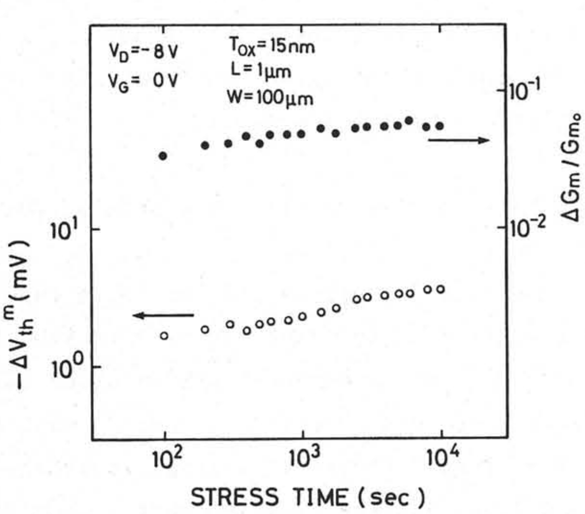

Fig. 3 Time dependence of V_{th}^m and G_m in n-channel MOSFET

3. Model and Discussion

In Figure 4, the shift of the tunnel threshold voltage ΔV_{th}^t is plotted against the total electric charge Q created by the band-to-band tunneling phenomenon. Though $V_D V_G$ is kept constant, ΔV_{th}^t strongly depends on V_D. This means that the electric field parallel to the Si-SiO_2 interface determines the extent of the degradation.

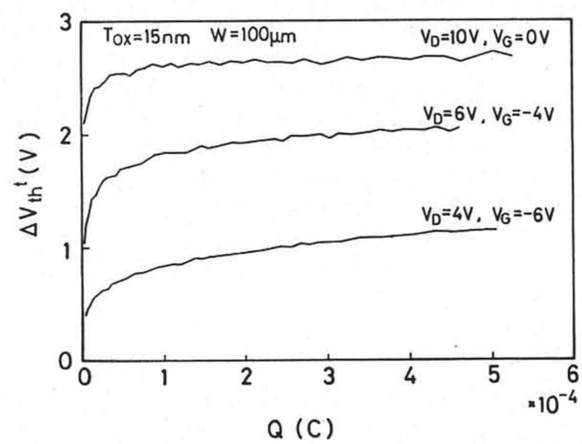

Fig. 4 ΔV_{th}^t is plotted against Q under V_{DG} =10V

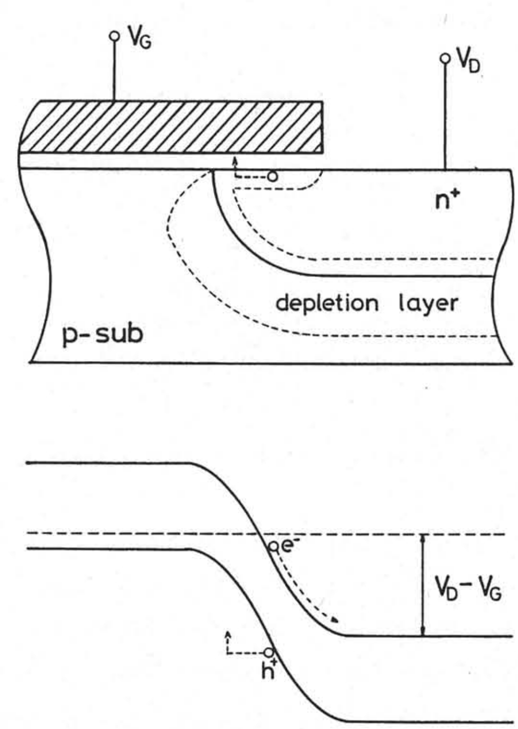

Fig. 5 Mechanism of hole injection into the gate oxide

Based on this data, a simple model of

the hole injection into the gate oxide has been proposed (see Fig. 5). The model is described below.

1)Due to the band-to-band tunneling phenomenon, electron-hole pairs are created in the gate-drain overlapped region.

2)The electrons are swept away to the drain electrode and the holes travel along the Si-SiO_2 interface towards the junction edge. Some of the created holes move without suffering any collision and obtain enough energy to surmount the Si-SiO_2 barrier.

3)As a result of elastic scattering, such holes are injected into the gate oxide and cause device degradation.

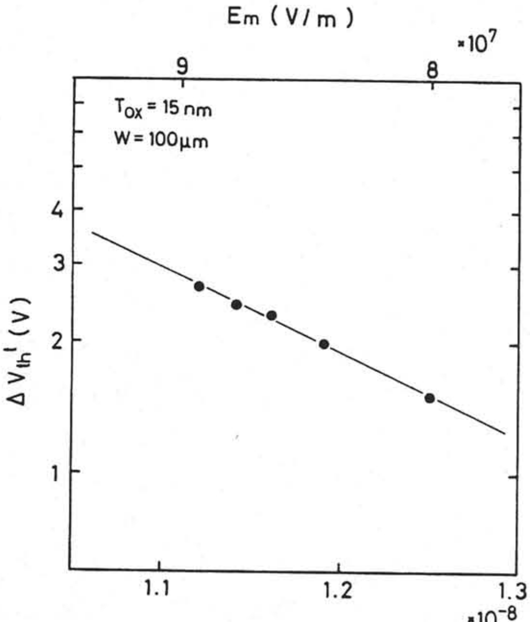

Fig. 6 log (ΔV_{th}^t) is plotted against $1/E_m$ in n-channel MOSFET

Hereafter, this model is treated analytically and verified quantitatively. The distance l that a hole must travel in the constant electric field E to obtain enough energy to surmount the Si-SiO_2 barrier is expressed as

$$l = \Phi_b / qE , \quad \text{(Eq. 1)}$$

where Φ_b is the Si-SiO_2 barrier height. If we take the maximum electric field E_m for E, the probability of a hole travelling l without collision is given as

$$P(l) \propto exp(-\Phi_b / q\lambda E_m) , \quad \text{(Eq. 2)}$$

where λ is the mean free path of the hole. Since the amount of injected holes Q_i is given by

$$Q_i \propto P(l)Q , \quad \text{(Eq. 3)}$$

ΔV_{th}^t is written as

$$\Delta V_{th}^t = Q_i / C_{ox}$$
$$\propto exp(-\Phi_b / q\lambda E_m), \quad \text{(Eq. 4)}$$

where C_{ox} is the capacitance of the gate-drain overlapped region.

In Fig. 6, log (ΔV_{th}^t) at $Q = 5\times 10^{-4}$ (C) is plotted against $1/E_m$. The data fall in a straight line and support our model as expressed by Eq. 4. In calculating E_m, a 3-D device simulator , CADDETH [6], was employed. From Fig. 6, the mean free path of a hole can be calculated to be 8nm. This value agrees well with the previously reported value of 4.5nm [7].

4. Device degradation for p-channel MOSFETs

In this section, the results for p-channel MOSFETs are given. In Fig. 7, the time dependence of V_{th}^t and I_{ld} is shown. Contrary to the case of n-channel MOSFETs, electrons are injected into the oxide and the electric potential of the gate electrode decreases. Therefore both V_{th}^t and I_{ld} decrease.

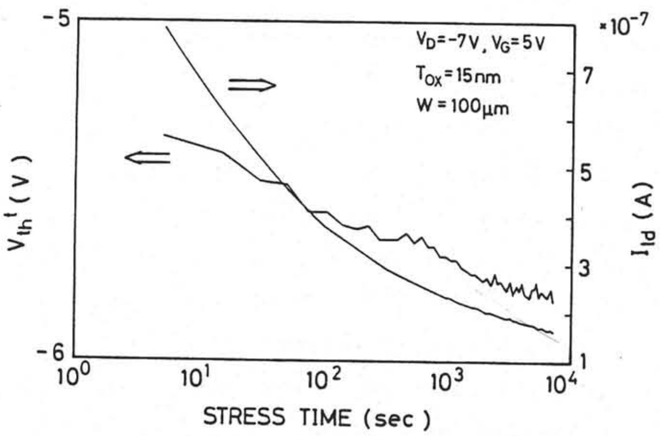

Fig. 7 Time dependence of I_{ld} and V_{th}^t in p-channel MOSFETs

The same arguement discussed for n-channel MOSFETs can also be applied to the p-channel case and the mean free path of an electron is calculated to be 10nm. This value is slightly larger than that of the hole and agrees well with the previously reported data of 6.2nm [7]. The validity of the model is verified by the fact that the mean free path of an electron and a hole obtained from our model are consistent with the previous values.

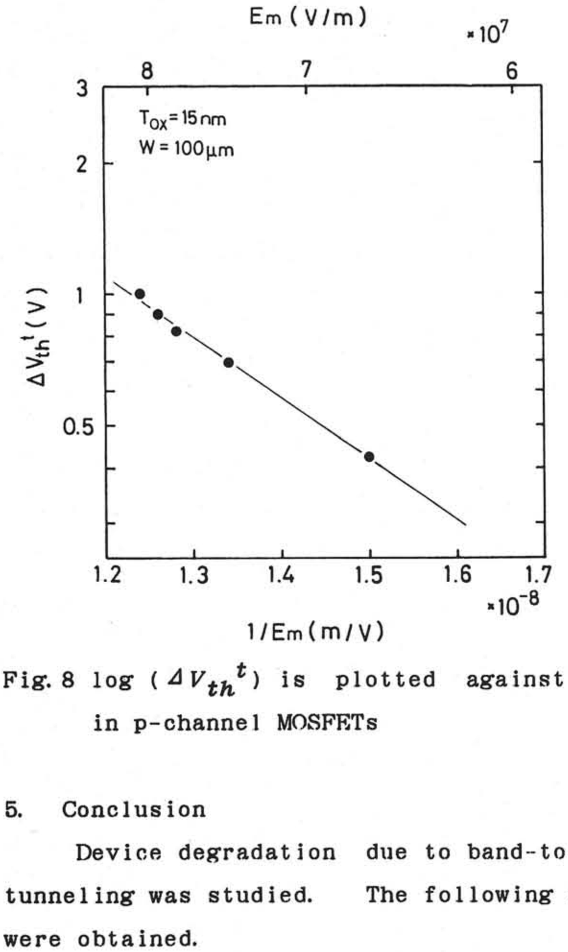

Fig. 8 log (ΔV_{th}^{t}) is plotted against $1/E_m$ in p-channel MOSFETs

5. Conclusion

Device degradation due to band-to-band tunneling was studied. The following facts were obtained.

(1) The carriers created by band-to-band tunneling can be injected into the gate oxide. Holes are injected in n-channel MOSFETs, while electrons are injected in p-channel MOSFETs. They cause shift in tunnel threshold voltage.

(2) Injected carriers bring about a new mode of device degradation in n-channel MOSFET. Namely, the MOS threshold voltage decreases and transconductance increases, which is opposite to the degradation caused by the 'hot' carrier effect.

(3) The injection model was proposed and verified quantitatively.

In addition to the 'hot' carrier effect, the band-to-band tunneling must be taken into consideration in developing scaled MOSFETs. To eliminate this degradation mode, it is necessary to reduce the maximum electric field, as is seen from Eq. 4. In this sense, reduced supplied voltage is very effective.

6. Acknowledgments

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7. References

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