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The Breakdown Behavior of Short-Channel CMOS Devices Under High-Frequency Operations

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Abstract--The dynamic breakdown behavior of short-channel NMOSFET's in bulk CMOS is investigated by applying an ac voltage to the gate terminal. It is found that a high-frequency gate clock induces an excess electron current which is proportional to the gate clock frequency and amplitude. With this excess electron current, the avalanche multiplication process near the drain region is strongly affected and the well-source bias is de-biased, leading to a different breakdown behavior. Moreover, the source junction could be turned on and the parasitic vertical and lateral transistors could be triggered. This also affects the dynamic breakdown behavior. It is found from the experimental results that the breakdown voltage could decrease at high-frequency operations. Thus in designing CMOS for high-frequency operations, the dynamic breakdown behavior has to be considered.

1. INTRODUCTION

It is known that the source-drain breakdown is one of performance limiting factors in scaled-down MOSFET's. Many literatures[1)-6)] have so far been devoted to the study of the source-drain breakdown under dc biases. It is found that such a breakdown behavior in the dc case is mainly caused by the avalanche multiplication due to high electric field and is strongly affected by the parasitic bipolar structures.

As the devices are more and more scaled down, the chip operation frequency is expected to be raised higher and higher. Thus it is necessary to investigate the device breakdown behavior under high-frequency ac operations, i.e., the dynamic breakdown behavior, as well as the dc breakdown behavior. For bulk p-well or dual-well CMOS, the dc breakdown behavior is much worse in n-channel MOSFET's and so is the dynamic breakdown behavior. Moreover, a n-channel MOSFET in bulk CMOS has another parasitic n^+-p-well-n-substrate bipolar transistor which also affects the breakdown behavior. Both effects of high-frequency operation and parasitic n-p-n bipolar structure have not yet been studied in any literature so far.

It is the aim of this work to investigate the breakdown behavior of n-channel MOSFET's in bulk CMOS, taking the above two effects into considerations. Some important findings and novel phenomena will be presented and analyzed.

2. EXPERIMENTS

The devices under investigation were fabricated with 1.5-μm twin-well CMOS technology. The effective channel width and length are 50 μm and 1 μm, respectively. The junction depth of source/drain is 0.32 μm for N-channel MOSFET's, 0.5 μm for P-channel MOSFET's. The resistivity of N-type substrate is 2 to 3 Ω-cm. The oxide thickness and the threshold voltage of N-channel MOSFET's are 250 Å and 1.014 V, respectively.

The experimental setups are shown in Fig. 1. A square wave (clock) with different frequencies and amplitudes, generated from a pulse/function generator, was applied to the gate terminal to simulate the ac operations.

The drain I-V characteristics were then measured by a parameter analyzer. The breakdown voltage was determined from the measured I-V characteristics. The effect of well (back-gate) biases on the breakdown behavior was evaluated by measuring the well currents under different well biases. To investigate the effect of n^+-p-well-n-substrate bipolar effect, all the measurements were performed under two different conditions: (a) The substrate is floating; and (b) the substrate is biased to V_{DD}.

Note that all the measured currents in the ac operations were their average currents. Thus the capacitance transient currents are not included.

3. RESULTS AND DISCUSSIONS

3.1 Excess Electron Currents

For n-channel MOS devices operated under a gate clock and a dc drain voltage well below the drain breakdown voltage, an extra current was measured at the well node in the floating-substrate case or at the substrate node in the biased-substrate case. The measured currents in the biased substrate case is shown in Fig. 2 where the current depends on gate clock amplitudes and frequencies. The origin of this current can be explained as follows.

As the gate voltage lowers to 0 V, the inversion electrons are dismissed instantly. Part of electrons moves to the drain/source regions whereas part of them moves to the substrate. Shortly after the dismissal, the gate voltage raises to a high voltage above the threshold voltage and the electrons have to form an inversion layer beneath the surface. The major source of inversion electrons is from the n^+ drain/source regions, instead of the substrate. This means that the dismissed electrons in the substrate can not totally respond to the gate voltage change and come back to the inversion layer. They become wandering electrons and have to be recombined quickly in the floating-substrate case and/or swept to the substrate in the biased-substrate case to retain the charge neutrality. An external current called the excess electron current, therefore, is generated as a result of electron recombinations or moving.

As the gate clock frequency is increased, more electrons fail to respond to the gate clock and thus are recombined and/or swept out. This leads to an excess electron current proportional to the clock frequency. Meanwhile, as the gate clock amplitude is increased and the frequency is fixed, the inversion electrons are increased by an amount proportional to the gate clock voltage amplitude. Thus the recombined or swept electrons and the excess electron current are also propor-

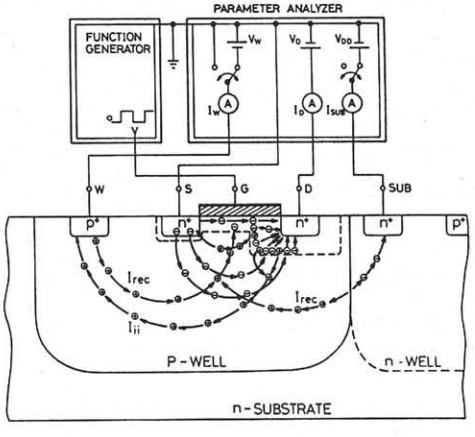

Fig. 1 Experimental setups to measure the dynamic breakdown of a CMOS device showing in cross-sectional view.

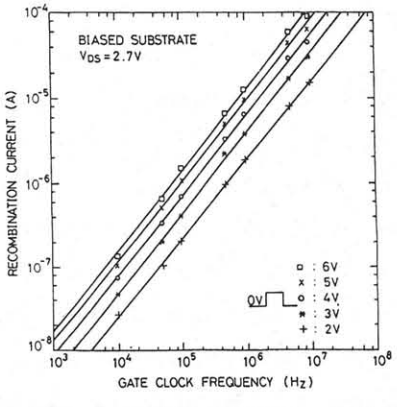

Fig. 2 Excess electron current as a function of gate clock frequency with different clock amplitudes.

tional to the clock voltage amplitude as shown in Fig. 3.

3.2 Substrate-Related Dynamic Breakdown

In the case of V_{DD}-biased substrate, the excess electron current flowing out of the power supply V_{DD} has the following effects:

(1) To turn on the source junction and make the breakdown behavior dominated by the parasitic lateral and vertical bipolar transistors;

(2) To retard the avalanche multiplication effect caused by the high drain electric field.

Fig. 4 shows the measured substrate currents as a function of the drain voltage with the gate clock frequency as a parameter. Due to the high substrate current at 10 MHz, the source junction is turned on suddenly which leads to a sharp increase of the substrate current at V_{DS}=2.8 V in Fig. 4. At sufficiently high drain voltage, avalanche multiplication occurs. Thus the source junction is more heavily turned on and the substrate current increases significantly.

The complete I-V characteristics with the amplitude of 10 MHz gate clock as the parameter are shown in Fig. 5 where the solid (dotted) lines represent the biased-(floating-) substrate case. In the case of biased substrate, the effects of parasitic lateral and vertical bipolar transistors and the avalanche multiplication effect lead to the snap-back phenomena. But they occur at a higher drain current because part of the holes generated from the avalanche multiplication recombines part of the excess inversion electrons in the substrate. Without the vertical bipolar action, the snap-back is less significant, as may be seen from Fig. 5.

Fig. 6 shows the breakdown voltages in the biased-substrate case as a function of gate clock amplitude at different clock frequencies. As the clock frequency increases up to 10 MHz, the breakdown voltage increases if the clock amplitude is low. This is due to the retarding effect of the excess electron current. As the clock amplitude increases, the breakdown voltage decreases first and then increases, resulting in C-shape breakdown characteristics[2]. At high clock amplitudes, a high clock frequency tends to have a lower breakdown voltage.

3.3 Well-Source Bias

To investigate the effect of well-source bias V_{WS} on the dynamic breakdown behavior, the well and the substrate currents (excess electron currents) at 10 MHz 6V gate clock were measured for different V_{WS} down to -2V as a function of drain voltages and they are shown in Fig. 7. It can be seen that excess electron currents gradually become the same for different V_{WS} at high drain voltages, especially in the case of floating substrate. The reason of this de-biasing phenomenon is that the high excess electron current at high clock frequency and amplitude produces a potential distribution within the well which shields the V_{WS} bias.

The breakdown voltages at 10 MHz gate clock and under different V_{WS} are plotted as a function of the gate clock amplitude in Fig. 8. It is seen that breakdown voltages for different V_{WS} tends to converge to the same value at high clock amplitudes due to the de-biasing effect of the high excess electron current.

4. CONCLUSIONS

It has been shown in this work that the dynamic breakdown behavior of a short-channel MOSFET under the operation of a high-frequency gate clock is quite different from its dc breakdown behavior. Under high-frequency operations, an excess electron current is generated which is proportional to clock frequency and amplitude. This current flows from the V_{DD}-biased substrate or the grounded well if the substrate is floating. It could

turn on the source junction, trigger the parasitic lateral and/or vertical bipolar transistors, retard the avalanche multiplication effect, and debias the well-source bias. Thus the dynamic breakdown voltage could be lowered if the excess electron current is too large at high frequencies. For a digital CMOS VLSI chip operated at high frequencies, therefore, the dynamic breakdown should be considered in performing the worst-case circuit device/process design.

In future works, theoretical models will be developed to characterize the excess electron current and the dynamic breakdown behavior. The effect of the excess electron current on other circuit speed performance and latchup immunity will also be addressed in the future.

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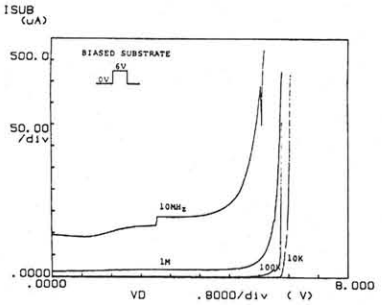

Fig. 4 Excess electron current flowing out of the V_{DD}-viased substrate as a function of drain voltage at different clock frequencies.

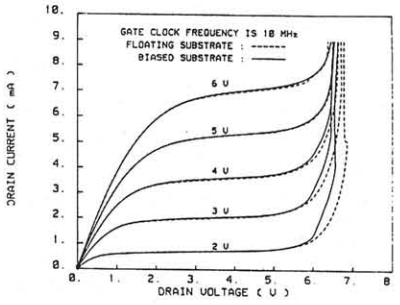

Fig. 5 I-V characteristics of the NMOSFET at 10 MHz gate clock, showing different breakdown curves in cases of floating- and biased- substrate.

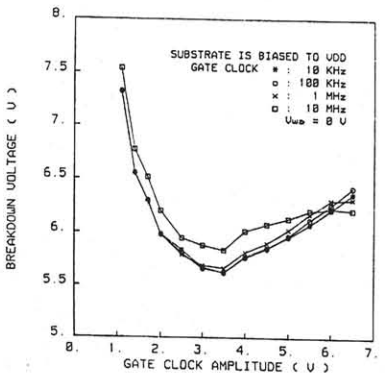

Fig. 6 Breakdown voltages in the case of biased substrate as a function of gate clock amplitude at different clock frequencies.

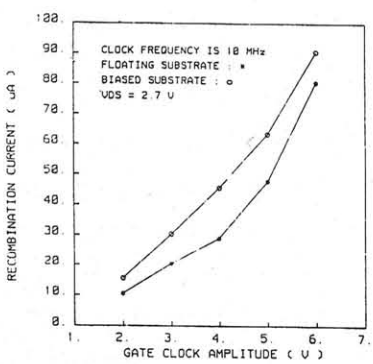

Fig. 3 Excess electron current as a function of gate clock amplitude at 10 MHz clock frequency.

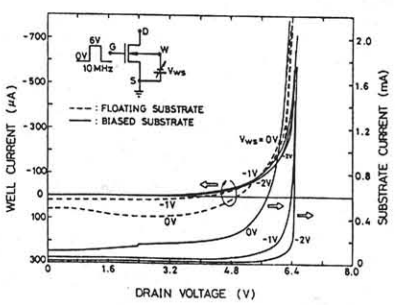

Fig. 7 Well and substrate currents as a function of drain voltage at 10 MHz gate clock under different well-source biases.

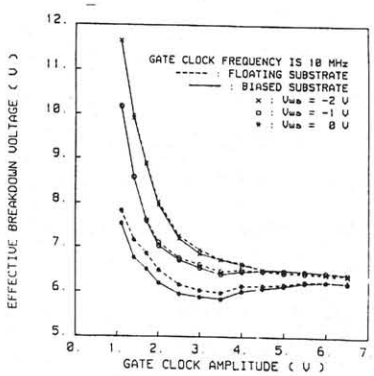

Fig. 8 Breakdown voltage at 10 MHz gate clock as a function of clock amplitude for different well-source biases.