Extended Abstracts of the 20th (1988 International) Conference on Solid State Devices and Materials, Tokyo, 1988, pp. 565-568

S-IIIB-5

**Invited**

# Metallization for ULSI

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The role of metallization is most important in determining speed performance, yield and reliability of devices as the technology advances toward ULSI. This paper is focussed on the planarization of interconnects, particularly hole filling, which in fact becomes the limiting factor of technology enhancement. Among a variety of candidates for the planarization, conformal CVD-W, selective CVD-W and bias sputtered AlCu are promising. The present status and limitations of these technologies are reviewed, and the future requirements are discussed.

## 1. Introduction

With the continued scaling down of VLSI 's interconnects can limit device performance, yield and reliability. In particular, problems with contacts in the conventional Al metallization process become quite serious, such as open or reliability failure of the Al interconnects due to high aspect ratio of contact holes and poor step coverage of the sputtered Al, increase in the contact resistance caused by Si precipitation, and degradation of the shallow junction characteristics by Al spiking. These problems in today's scaled-down devices strongly require new materials and processes which planarize the contact holes with excellent characteristics and reliaibility.

A variety of candidates for the planarization of interconnects (hole filling) have been proposed as summarized in Table 1. This paper reviews and discusses recent advances in the planarization technologies.

## 2. Conformal CVD

Completely conformal deposition can provide flat surfaces because films deposited on sidewalls of holes and grooves will combine with one another to fill them. The conformal CVD planarization is quite attractive since it requires only a single deposition process which involves both hole filling and interconnect metallization. In order to obtain conformal coverage, low pressure CVD technique is used under the condition that the deposition rate is limited by surface reaction, not by mass transport.

Much interest becomes to be taken to blanket CVD-W [1,2] instead of Al [3,4], conventional material, because CVD-Al has problems of film quality, low deposition rate and difficulty in adding impurities. Fingure 1 shows a SEM photograph where blanket W is deposited on Si grooves. It is seen that the grooves are completely filled by the W film without any keyhole (void). Another important feature is its high

electromigration resistance, whose lifetime is longer than that of Al interconnect by about 15 orders of magnitude[5]. The adhesion problem between W and SiO2 can be prevented by adding a thin layer between them such as TiW and TiN, which can also ensure junction characteristics and high-temperature resistance (about 900°C).

The resistivity is relatively high (about 10 $\mu\Omega$-cm) compared with that of Al. In order to reduce the resistance, Al/W structure has been reported [6]. Another problem is its surface morphology as seen in Fig.1. Since the rough surface makes it difficult to detect an alignment marker during lithography, it will be required to optimize the deposition condition.

## 3. Bias Sputtering

Planarized metal layers can be achieved by bias sputtering under high resputtering condition. Al [7] and Mo [8] films have been filled in contact holes. The deposition rate, however,is very low and is estimated to be less than 0.14$\mu$m/min for Al [9], since flat surfaces require etching of the deposited metal in quantities.

Planarization can be obtained by another mechanism due to substrate heating (400~500° C) and Ar ion irradiation, resulting in a plastic deformation of Al film to fill the contact holes [10]. In this case the depcsition rate hardly decreases to be 0.5 $\mu$m/min [11]. Figure 2 shows a SEM photograph of the step coverage. Barrier layers seem to be necessary in order to prevent Al/Si interactions and to provide good filling property. The bias sputtering method has an advantage over other methods, since it employs familiar process except for the slight modification of a sputtering system.

A problem encountered in this technique is the degradation of film quality. The alignment of the interconnect is difficult because of the low reflectivity due to surface roughness. Furthermore, in the case of AlSi the lifetime of electromigration is remarkably reduced compared with the conventional film [12]. Most recently, however, it has been reported that the lifetime is improved by using AlCu films [13], indicating the importance of materials. It will be needed to study the limit of applicable aspect ratio.

## 4. Selective Deposition

A variety of metal films can be selectively deposited on Si, silicide and other metals, but not on dielectric materials by CVD technigue [14]. Selective CVD-W has been exciting interest, since recently a novel process by using silane reduction of tungsten hexafluoride has been reported [15,16]. The silane-reduction process can provide a very high deposition rate of 0.6 $\mu$m/min compared with the conventional hydrogen-reduction process of several 0.01 $\mu$m/min. Figure 3 shows a SEM

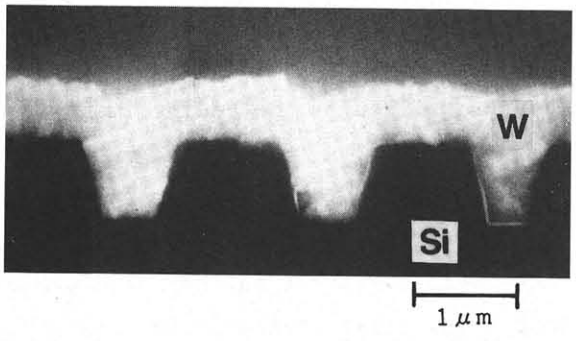


Fig.1 Step coverage of conformal CVD-W.

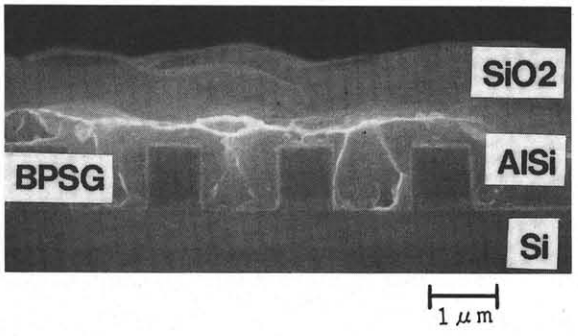


Fig.2 Step coverage of bias-sputtered AlSi.

picture of contact holes filled by selective CVD-W. The process can suppress undesirable reactions between W films and Si substrate such as encroachment and wormholes, resulting in excellent electrical characteristics. The W films also can prevent the Si precipitation due to AlSi interconnects, and then ensure the stable contact resistance particularly for small contacts even after heat treatment at 500°C.

The fatal problem in this method is not to understand the mechanism of selective deposition clearly. In a fabrication process it is difficult to completely fill all holes with different depth, although it has been reported that holes with different depth can be filled by using the deposition-rate dependence on underlying materials [17]. Therefore, device structures must be optimized, or the film thickness must be chosen to be the most shallow depth.

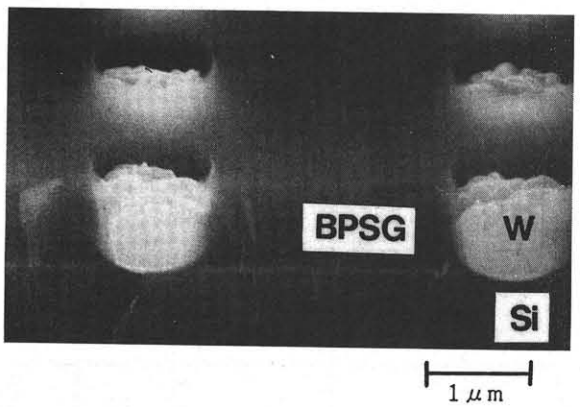


Fig.3 Hole filling by selective CVD-W.

## 5. Summary

Planarization technologies of interconnects, particularly hole filling, have been reviewed. Although many kinds of methods have been prorosed, comformal CVD, selective CVD and bias sputtering are promising candidates for future devices to overcome severe metallization problems. In order to apply them in a mass production, further advances are necessary regarding planarization mechanism, film characteristics, controllability, process compatibility and throughput.


## Acknowledgments

The anthor would like to thank Drs. K.Shibayama, N.Tsubouchi and S.Nagao for their discussion and encouragements.


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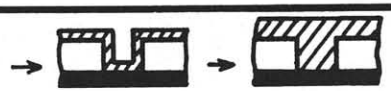
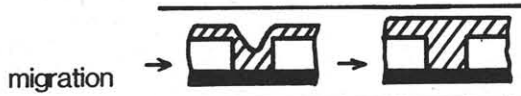
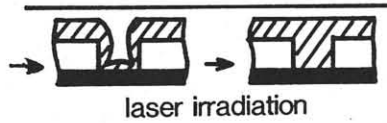
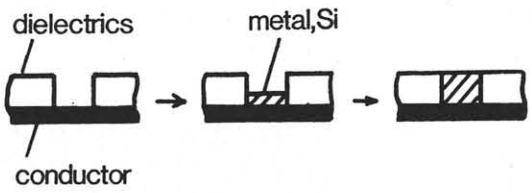
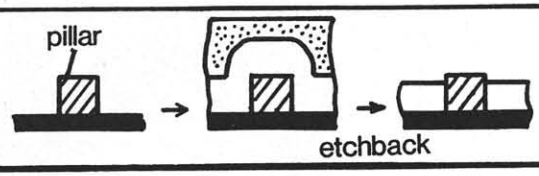
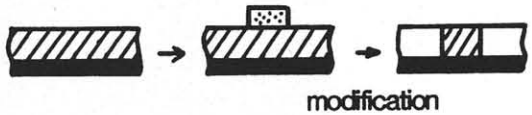
Table 1 Planarization (hole filling) technologies of interconnects.

| TECHNIQUES | | SCHEMATIC CROSS SECTIONS | ADVANTAGES | PROBLEMS |
|---|---|---|---|---|
| conformal deposition | CVD |  | simple familiar process | film quality |
| material deformation | bias sputtering |   | conventional process except for modification of sputtering system | low deposition rate |
| | |   | | limit of applicable aspect ratio |
| | laser irradiation |   | relatively simple | controllability film quality |
| selective deposition | CVD |   | well investigated | not for different depth |
| | epitaxial growth | | established apparatus | not for both n and p layers at the same time |
| | plating | | applied to other fields | process compatibility |
| combined process | lift-off |   | combination of conventional techniques | complicated controllability |
| | pillar |   | | |
| material modification | anodic oxidation |   | simple not need of hole formation | controllability dielectrics quality |
| | ion implantation | | | |