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A New CMOS Structure Using a Transistor on a Lateral Epitaxial Silicon Layer

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A new CMOS (CMOS-TOLE : Transistor On a Lateral Epitaxial silicon layer) structure has been developed to achieve high packing density and high speed. The CMOS-TOLE structure is characterized by the source(S)/drain(D) regions and part of the channel regions adjacent to S/D regions which are formed on epitaxial silicon layer on insulator film. It has the following advantages. (1) Reduction of the isolation width without loss of latch-up immunity and (2) parasitic capacitance reduction of S/D regions. These advantages have been verified using test devices including 25-stage ring oscillators.

1. Introduction

Device dimension reduction and parasitic capacitance reduction are very important requirements for producing future CMOS ULSIs that have high packing density and high speed performance. However, it is difficult for the conventional bulk CMOS structure to satisfy these requirements because (1) its isolation width between p- and n-channel transistors cannot be reduced without loss of latch-up immunity, and (2) parasitic capacitances, such as the boundary component of a junction capacitance and a wiring capacitance, are not reduced, even when device dimensions are scaled down.

This paper proposes a new CMOS structure, which employs a transistor on a lateral epitaxial silicon layer[1] technique and is called CMOS-TOLE. This paper describes the CMOS-TOLE structure and its fabrication process. It also presents some experimental results indicating that the CMOS-TOLE can satisfy the above-mentioned requirements.

2. CMOS-TOLE structure

Figure 1 shows a cross sectional view of the twin-well CMOS-TOLE structure. The CMOS-TOLE is formed partly on insulator film. The source(S)/drain(D) regions and part of the channel regions adjacent to the S/D regions are formed on epitaxial silicon layers, which are on thick oxide insulator film. The middle part of the channel regions are connected to the bulk silicon substrate. The transistor areas are surrounded by vertical sidewalls formed with insulator film.

The CMOS-TOLE structure, then, has the following advantages:

(1) The isolation region width can easily be reduced. There are two reasons for this.

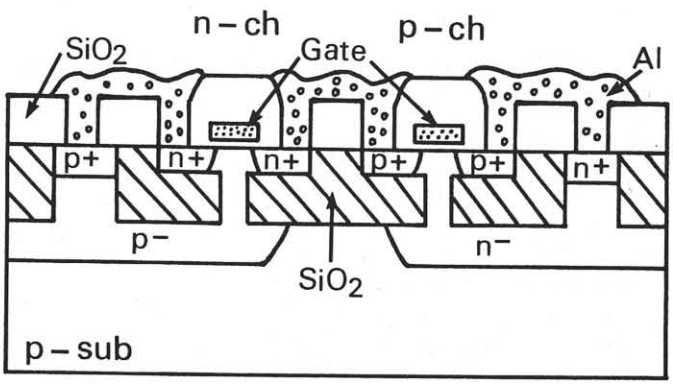


Fig. 1 CMOS-TOLE structure.

The first is that this width is determined by size of the resist pattern. The second is that high latch-up immunity may be achieved even for a narrow isolation region because shape of the oxide-film between the p- and n-channel transistors permits a long latch-up current path through the lateral npn transistor.

(2) The parasitic capacitance between the S/D regions and the silicon substrate can be easily reduced while maintaining a flat surface because the oxide film thickness beneath the S/D regions can be easily increased with epitaxial lateral overgrowth (ELO) [2] and preferential polishing (PP) [3] techniques. In this respect, CMOS-TOLE is different from BOMOS [4], LID [5] and SPEG [6]. The parasitic capacitance between the wiring and the silicon substrate can be also reduced.

(3) Stable dynamic transistor action may be obtained because the substrate is not electrically floating. This aspect is important to the application of CMOS-TOLE to dynamic low power dissipation circuits.

3. Fabrication Process

Figure 2 shows the steps of the CMOS-TOLE fabrication process. ELO and PP techniques are employed to form a partial SOI structure. Boron and phosphorus ions are implanted three times to form the p- and n-well regions, respectively. The first implantation is done on the silicon substrate. (Fig. 2, a) This implantation makes the connection layer between the well-region beneath the channel region and the well-contact region. A 600nm thick field oxide film is thermally grown on the silicon substrate. (Fig. 2, b) Section cut-outs at two levels on the oxide film are formed by two oxide film etchings with the resist as a mask. The upper cut-out shape determines the transistor area and the channel width. The lower cut-out shape determines the seed area. The bottom of the upper cut-out determines the S/D junction depth (200nm). After cut-out formation, a second implantation is performed on the silicon substrate in the seed area to control impurity concentration in the deep region of the epitaxial silicon layer. (Fig. 2, c) A 5 μm thick epitaxial silicon is selectively grown from the exposed silicon substrate in the seed area using the ELO technique. (Fig. 2, d) The epitaxial silicon is polished with the PP technique, which leaves it in the two- level cut-out sections only. With this step, a flat surface is obtained, and the transistor areas are automatically isolated. A third implantation is then done to the epitaxial silicon layer to determine

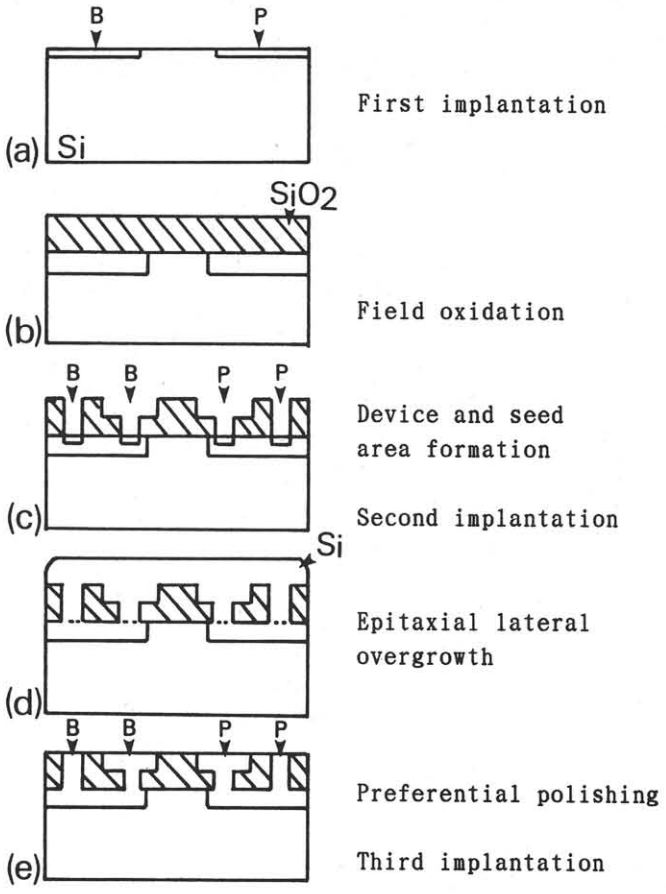
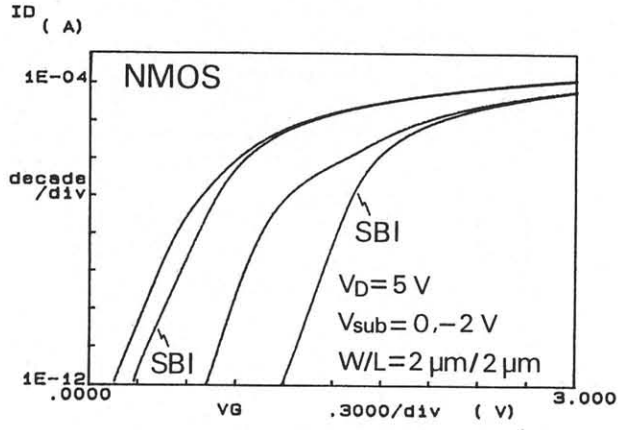
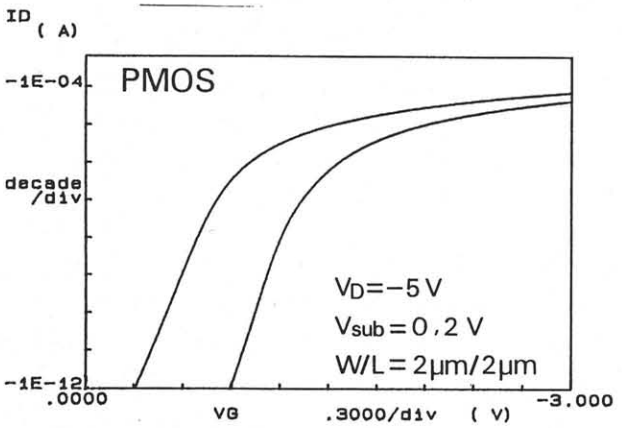


Fig. 2 CMOS-TOLE fabrication steps.

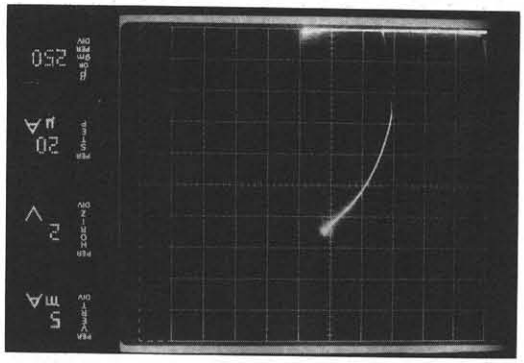


(a) N-channel transistor

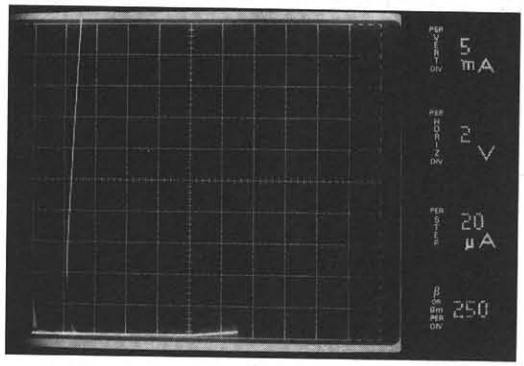


(b) P-channel transistor

Fig. 3 Subthreshold characteristics.
SBI : Sidewall Boron Implant



(a) CMOS-TOLE



(b) non-CMOS-TOLE

Fig. 4 Latch-up characteristics.

the transistor characteristics. (Fig. 2, e) After the third implantation, the gate electrodes, the S/D regions, the contact holes, and the aluminum wirings are formed.

4. Electrical Characteristics

Figure 3 shows the subthreshold characteristics of the n- and p-channel transistors. The clearly observable double hump for the n-channel transistor is caused by the formation of sidewall parasitic channel. We have confirmed that this double hump can be eliminated by increasing the threshold voltage at the sidewall parasitic channel region with a sidewall boron implant (SBI), as shown in Fig. 3, (a).

Figure 4 compares the latch-up characteristics of the CMOS-TOLE structure with those of a non-CMOS-TOLE structure which does not has a oxide film below the S/D regions. These CMOS test devices were fabricated with a 2 μm design rule. No high holding voltage was measured in these test samples because the first implantation dosage for them was low. However, these results demonstrate that the CMOS-TOLE structure is effective for enhancing latch-up immunity.

25-stage ring oscillators of both the 1 fan-in and 3 fan-ins type were made using the CMOS-TOLE and non-CMOS-TOLE structure. The W/L for the n-channel transistor was the same size as that for the p-channel transistor, 6 μm/2 μm. Figure 5 shows measured delays as a function of the power supply voltage. With a 5V power supply, a per-stage delay increase between 1 fan-in and 3 fan-ins for the CMOS-TOLE was 1/5 of that for the non- CMOS-TOLE. The reason for this is that the parasitic capacitance of

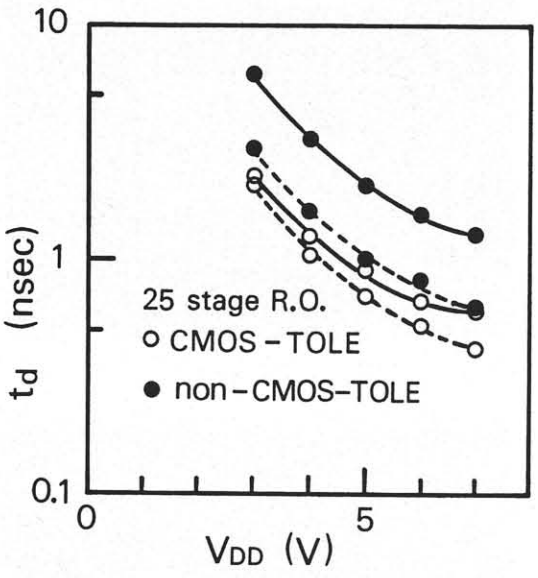


Fig. 5 Ring oscillator gate delay, 3 fan-ins and 1 fan-out with solid line, 1 fan-in and 1 fan-out with dashed line. Both devices : W/L=6/2 (μm).

the CMOS-TOLE in the fan-in region, which mainly consists of S/D junction capacitance, is smaller than that for the non-CMOS-TOLE.

Fig. 6 shows the drain currents for MOS-TOLE and non-MOS-TOLE without the oxide film below the S/D regions. An MOS-TOLE, like an MOS transistor with an LDD structure, provides higher drain-breakdown voltage than a conventional MOS transistor. This may be explained by the fact that the electrical field near the drain region of the TOLE structure is weakened by its partial SOI structure.

5. Conclusion

A new CMOS structure, the CMOS-TOLE has been proposed. It has been found to be effective for improving latch-up characteristics and increasing drain-breakdown voltage. It has been confirmed with 25-stage ring oscillators that parasitic capacitance, which cannot be reduced for a bulk CMOS structure, can be reduced for the CMOS-TOLE.

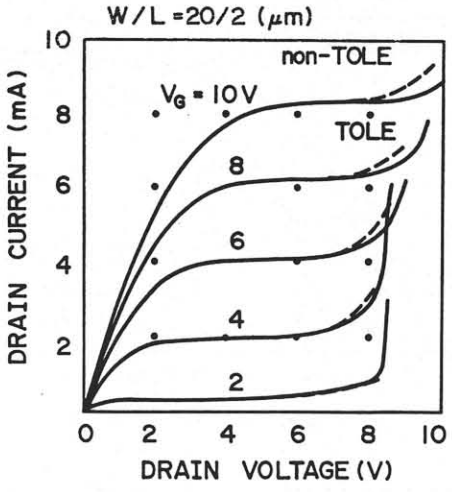


Fig. 6 Drain currents for MOS-TOLE (solid line) and MOSFET (dashed line) without SOI part(non-TOLE).

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