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A Novel Storage Capacitance Enlargement Structure Using a Double-Stacked Storage Node in STC DRAM Cell

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This paper describes a novel storage capacitance (Cs) enlargement structure for a stacked capacitor (STC) DRAM cell. The Cs is 51 fF/cell with a 5-nm SiO_2-equivalent-thickness dielectric film in a 4.2-μm^2 cell area. This is 1.7 times larger than a conventional STC cell. The capacitor dielectric film formed on the double-stacked storage node ensures reliable memory operation. This storage capacitance enlargement structure is promising for 16 Mbit DRAMs and beyond.

INTRODUCTION

It has become necessary to adopt three-dimensional cell structures such as stacked capacitor (STC) cell structure[1][2] and trench capacitor cell structure[3], since the memory cell size in DRAMs has been decreasing. The trench capacitor cell, in particular, is considered promising for 16 Mbit DRAMs, because it can realize larger storage capacitance than STCs. However, the advantage of the STC cell is that conventional VLSI technology can be readily applied to its fabrication.

The key issue concerning STC cell is to obtain enough Cs in a small cell size to operate with high reliability.

This paper proposes a novel storage capacitance (Cs) enlargement structure having a double-stacked storage node in an STC cell. The characteristics of the capacitor dielectric film formed on the double-stacked storage node is discussed. Also, charge retention characteristics of the memory cell with this structure is compared with that of the conventional STC cell.

PROCESS STEPS OF DOUBLE-STACKED STORAGE NODE STRUCTURE

A large Cs is achieved by double-stacking of the storage node electrode, and by making a recessed side-wall, resulting in a substantial increase in storage node surface. Key fabrication steps are described in Fig.1. (a) 1st a storage node is formed on a transfer MOS transistor (word-line). (b) Si_3N_4 and SiO_2 layers are deposited and then a via-hole is opened. Then the 2nd storage node is formed. (c) The SiO_2 and Si_3N_4 layers are removed by wet-etching, forming a recessed side-wall. Si_3N_4 acts as an etching stopper when SiO_2 is removed. (d) A capacitor dielectric film is grown on the recessed surface and then a plate-electrode is deposited. Although there are extra process steps, no additional mask is needed for this new process.

A cross-sectional SEM photograph of this storage node structure is shown in Fig.2. The recessed side-wall is clearly visible. The substantial increase in surface area of the storage node

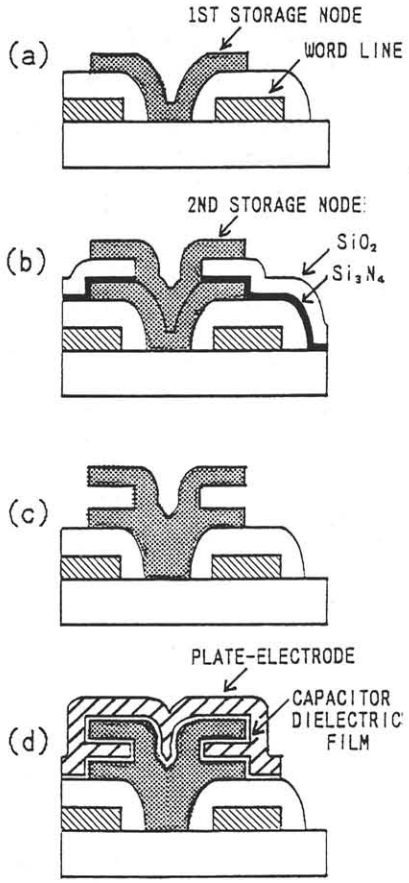

Fig.1 Key fabrication steps of double -stacked storage node structure in a STC cell

dramatically increases the storage capacitance.

One of the disadvantages of this structure is its height. Thus, because of the step between the memory cell array and the peripheral transistors, focus depth margin of a projection aligner is deteriorated. However, this problem can be solved by making a recessed area on the substrate where the memory array is located. This recessed area can be made by selective oxidation and subsequent SiO_2 removal[4].

ELECTRICAL CHARACTERISTICS OF THE DOUBLE -STACKED STORAGE NODE CAPACITOR

(1)storage capacitance

The distance between the first and the second poly-Si nodes of the double

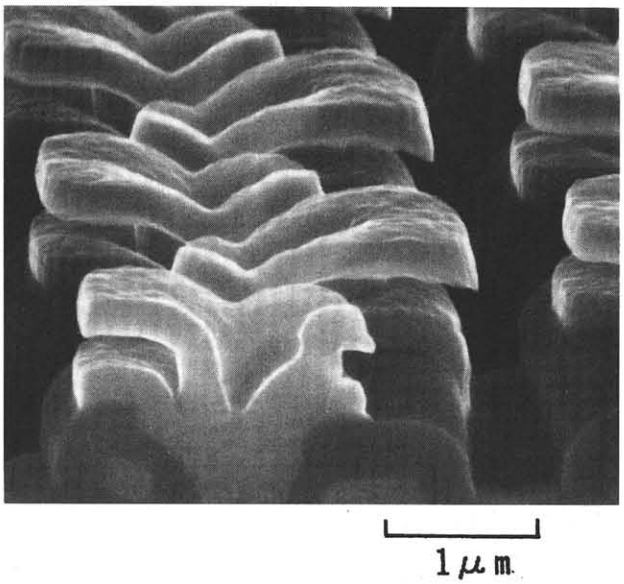

Fig.2 Cross sectional SEM photograph of double-stacked storage node

-stacked structrue is only 200nm. If this space is filled by the poly-Si plate, even phosphorus cannot diffuse to the interface. Thus, the lack of phosphorus concentration near the interface causes the depletion region in the plate -electrode to spread, thus reducing capacitance. In this experiment, two -step poly-Si deposition and phosphorus doping was adopted. Figure 3 compares the C-V characteristics of the storage capacitance with and without the two-step doping. It is clear that the capacitor without two-step doping is strongly voltage-dependent, also, about 30 % capacitance difference is observed. Thus, two-step doping was found effective in maintaining storage capacitance.

Figure 4 shows the storage capacitance of a 4.2-μm^2 STC cell using the present double-stacked storage node. The Cs of the conventional storage node structure is also given for comparison. This new structure gives a Cs of 51 fF/cell with the 5-nm SiO_2-equivalent-thickness dielectric film. Even an 8- or 9-nm film, used in 4 Mbit STC cells, gives more than

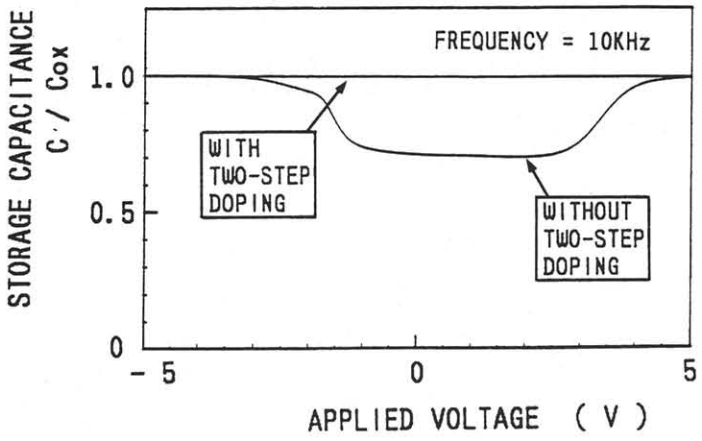

Fig.3 C-V characteristics of the storage capacitance

30 fF/cell, which is suffcient for memory operation. These results indicate that the present structure is very effective for increasing Cs in a very small STC cell.

(2)Dielectric breakdown strength

Figure 5 compares the critical field distributions of planar and double -stacked storage node capacitors. The critical field is corresponding to a 1 μA/cm^2 leakage current. It should be noted that the distribution of the double -stacked capacitor is as same as that of the planar capacitor [5]. Average critical field of the double -stacked storage node capacitor is about 7.0MV/cm, which is suffcient for memory operation.

MEMORY OPERATION

An experimental 2-kbit memory array was fabricated utilizing the above technologies, and successful memory operation was observed. The memory cell was a 4.2-μm^2 self-aligned isolated plate STC cell with 0.6 μm pattern delineating technology [6]. Transfer gate pitch and bit-line pitch were 1.3 μm and 1.6 μm, respectively. Charge retention characteristics of the memory cells with and without this double stacked structure

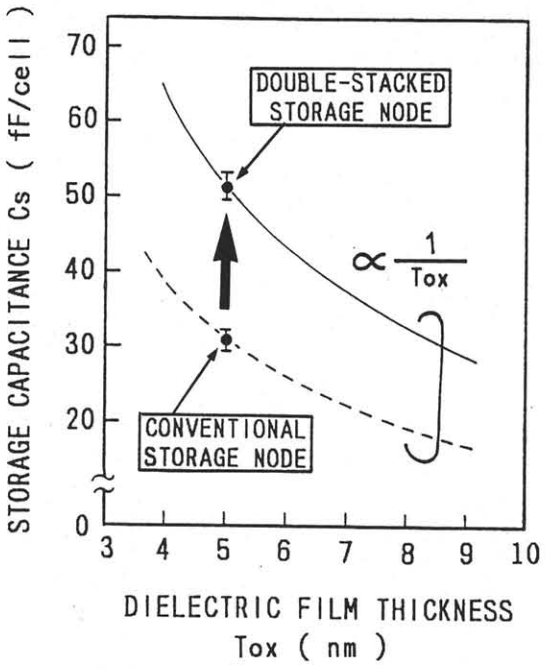

Fig.4 Storage capacitance, comparison between double-stacked storage node and conventional storage node

are shown in Fig.6. The measurement temperature was set 40℃. Retention time, defined as the time at which 50 % of the bits failed, was evaluated to be 15 seconds for the cell with the double -stacked capacitor. 1.5 times larger

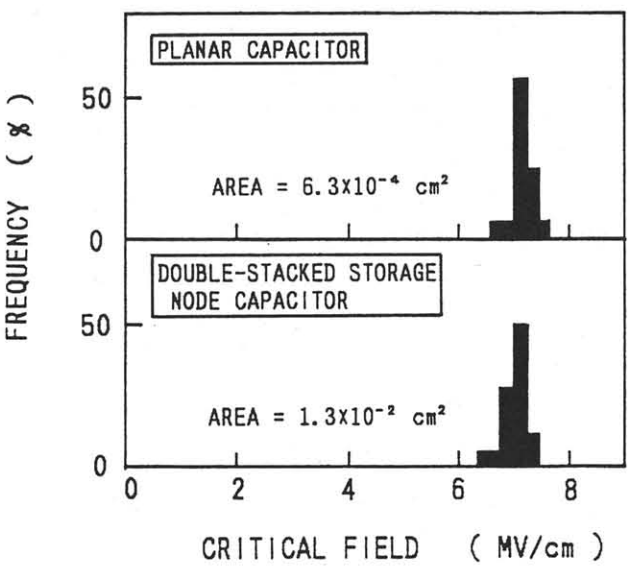

Fig.5 Critical field distributions of planar and double-stacked storage node capacitors

retention time than the conventional STC, was observed in accordance with the increase in storage capacitance.

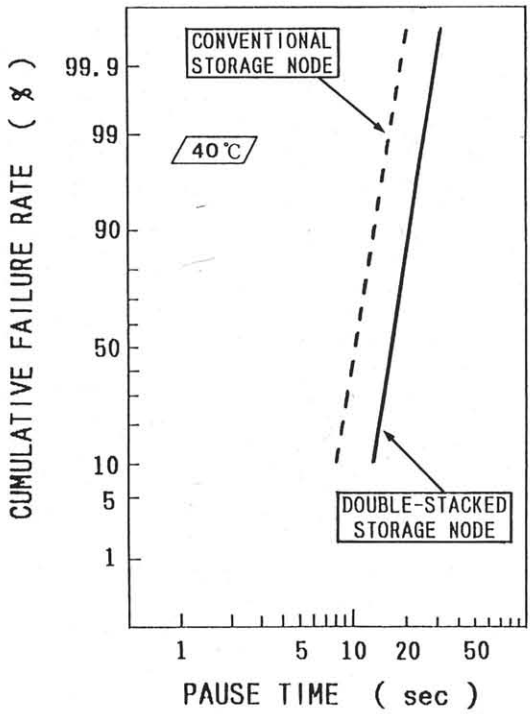

Fig.6 Charge retention characteristics, comparison between double -stacked structure STC and conventional structure STC

POTENTIALITY OF DOUBLE-STACKED STRUCTURE FOR 64 MBIT DRAMS

The effective capacitor area of the double-stacked structure is evaluated to be 7.58 - μm^2, since the Cs is 51 fF with a 5 -nm SiO_2 -equivalent -thickness dielectric film. Therefore, the ratio of storage capacitor area to cell area becomes 1.82. This is much larger than the value obtained in planar cells (typically 0.4). The trend of memory cell size reduction indicates that a cell of less than 2- μm^2 is necessary for 64 Mbit. If the double-stacked structure is applied to this 2- μm^2 cell, capacitor area of 3.64- μm^2 can be realized. This means that storage capacitance of 30 fF/ cell, which is necessary for favorable memory operation, can be obtained with 4.1 -nm thickness dielectric film. These considerations strongly indicate that an STC cell with this kind of storage node structure has remarkable potential, even for 64 Mbit DRAMs.

CONCLUSION

A novel storage capacitance (Cs) enlargement structure, using a double -stacked storage node in an STC cell is proposed. The Cs is 51 fF/cell with a 5 -nm SiO_2 -equivalent -thickness dielectric film in a 4.2- μm^2 cell area. This is 1.7 times larger than for a conventional STC cell. The capacitor dielectric film formed on the double-stacked storage node provides reliable memory operation. The charge retention characteristics were observed to improve using this double -stacked storage node. The STC cell using a double-stacked storage node is thought to have potential for forthcoming 16 Mbit DRAMs and beyond.

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