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### Invited

## Limited Reaction Processing: Growth of Si-Ge/Si for Heterojunction Bipolar Transistor Applications

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Limited Reaction Processing (LRP) is a technique for growing semiconductor and insulator layers in a single wafer configuration. The process is particularly well suited to the growth and processing of column IV strained layer structures, such as strained  $\mathrm{Si}_{1-x}\mathrm{Ge}_x$  on Si. Such alloys provide significant band gap discontinuity and may play a critical role in the development of column IV-based heterostructure devices. We will discuss the growth and material properties of  $\mathrm{Si}_{1-x}\mathrm{Ge}_x$  layers and their application in the development of high quality  $\mathrm{Si}/\mathrm{Si}_{1-x}\mathrm{Ge}_x/\mathrm{Si}$ heterojunction bipolar transistors.

#### THE LRP CYCLE

A single LRP cycle begins by establishing an appropriate flow of reactive and carrier gases over a cool wafer. Using lamp heating, the wafer is then rapidly heated to the desired temperature, inducing a chemical reaction on the wafer surface. The reaction proceeds at this temperature for the desired time, after which it is terminated by switching off the lamps. The wafer then cools rapidly and the This technique limits reaction ceases. the thermal exposure of the wafer and permits the deposition and epitaxial growth of a variety of different layers successively, without removing the wafer from the reaction chamber. LRP provides the capability to use the highest processing temperature for a given amount This flexibility of thermal exposure. allows for improved growth optimization of qualities such as defect density and dopant activation for each layer in a multi-layer structure.

### REVIEW OF SILICON PROCESSING

A number of experiments have demonstrated the ability of LRP to improve the fabrication process control of silicon based structures<sup>1-7)</sup>. Early results showed that intrinsic epitaxial silicon layers can be grown on heavily doped (n+ and p+) silicon substrates with dopant transition widths comparable to those obtained by molecular beam epitaxy Alternating undoped and boron (MBE). doped regions (i.e., i/p+/i/p+...) with dopant transition widths of less than 50Å/decade have been achieved with LRP. Hole mobilities in p+ epitaxial films are comparable to those measured in bulk Using selective epitaxial material. silicon growth combined with oxidation and polysilicon gate deposition, formation of in-situ MOSFETS has been demonstrated.

For LRP silicon epitaxy, interfacial carbon and oxygen concentrations below the detectability limit of secondary ion mass spectroscopy (SIMS) have been obtained. Surface oxides which tend to form during the growth-interrupt period are removed by "scrubbing reactions" that occur during the growth of the first few atomic layers of epitaxial silicon. Dichlorosilane promotes a particularly effective surface scrubbing reaction and was used as the silicon source gas in all of the  $Si_{1-x}Ge_x/Si$  work described in the following sections.

Since an interrupted growth interface can be contained within the space charge region of a pn junction, epitaxially grown junctions provide a stringent test of the device quality of LRP layers and interfaces. For Si junctions, forward current ideality factors of  $1.01 \pm 0.003$  have been obtained over more than 7 decades of current, extending down to 1 pA for diode areas in the range of  $10^{-3} - 10^{-5}/$ cm<sup>2</sup>. Very low reverse current densities (less than 3.5 nA -  $cm^{-2}$  at -5 V) and high breakdown slopes of 26-30 dec/V have also been achieved.

### LRP GROWTH OF Si1-xGex/Si

LRP is particularly well-suited to the growth and processing of epitaxial strained layers such as Si1-xGex/Si. The minimum thermal exposure helps to avoid strain relaxation. The ability to grow a high quality epitaxial buffer layer (of Si) is also an advantage, since it has been shown that defects in buffer layers can act as misfit dislocation nucleation sites in strained layer epitaxy. In addition, thin layers, on the order of 50Å, can be readily grown, with interface abruptness on the order of several monolayers under appropriate conditions.

# MISFIT DISLOCATION FORMATION AND THERMAL STABILITY

The onset of misfit dislocation formation during LRP growth of strained Si<sub>1-x</sub>Ge<sub>x</sub>/Si has been studied on both boron-doped  $(10^{19}/cm^3)$  and undoped layers. Defect densities were measured directly using a combination of x-ray topography and plan-view transmission microscopy. At a growth temperature of 625°C, LRP samples with a Ge fraction of 0.22, are dislocation-free at thicknesses up to 550Å. Misfit dislocations are observed at a thickness of 600Å, which is about 5 times the value predicted by equilibrium theory. These results are comparable to reports in the literature for MBE-grown films<sup>8)</sup>, which suggests that the growth technique does not dominate the onset of misfit dislocations during growth.

Annealing studies on 550Å thick films grown both by MBE and LRP were also conducted to determine the probable effects of subsequent processing steps. The data suggests improved thermal stability for LRP compared to MBE samples at temperatures less than 850°C. We have also observed that an epitaxial Si cap of sufficient thickness enhances the thermal stability of these strained layers.

### HETEROJUNCTION DEVICES

 $Si/Si_{1-x}Ge_x/Si$  heterojunction bipolar transistors (HBTs) are being investigated as a means of extending the performance limits of Si bipolar technology. Both calculations and measurements show that the total bandgap discontinuity between  $Si_{1-x}Ge_x$  and Si can be increased by using strained

Si<sub>1-x</sub>Ge<sub>x</sub>. Our first experiments on heterojunction devices involved fabrication of pn Si<sub>1-x</sub>Ge<sub>x</sub>/Si diodes. These devices provided measurements of the valence band discontinuity between Si and Si1-yGey, and formed the basis of a comparative study of defect structure and electrical behavior. Diode ideality factors of 1.01 in the forward current characteristics were fabricated, with Si<sub>1-x</sub>Ge<sub>x</sub> p-type regions of 520, 840 and 1160Å. Nonideal recombination appeared at low bias for 2000Å thick Si1-gGe, layers; and such recombination completely dominates the characteristics of diodes in which the Sil-xGex layer is 3000Å thick or more. The reverse bias characteristics are consistent with those at forward bias. The temperature dependence of the diode saturation current for these devices provides a direct device measurement of the valence band discontinuity between Si and Si<sub>10x</sub>Ge<sub>x</sub>. The results of these measurements will be discussed and shown to agree well with published calculations.

### HETEROJUNCTION BIPOLAR TRANSISTORS

The collector, base and emitter layers for a heterostructure transistor with Si collector and emitter layers and a Si<sub>l-x</sub>Ge<sub>x</sub> base were grown sequentially in the LRP apparatus. Base and emitter contacts were fabricated by appropriate implant and rapid thermal Details of the device anneal cycles. fabrication are described elsewhere<sup>9)</sup>. The Ge fractions in the base layers varied from 15-31%. Si control devices (BJTs) with base layers grown at 850°C were also fabricated. Figure 1 shows SIMS data for a Si0.69Ge0.31 sample with standard emitter and collector

layers and a base doping level of  $7 \mathrm{x} 10^{18} / \mathrm{cm}^3.$ 

Figure 2 is a Gummel plot which compares the current characteristics for an HBT (solid curves), to those of the Si control device (dashed curves). The HBT has a 200Å-thick Si0.69<sup>Ge</sup>0.31 base, doped to  $7 \times 10^{18} \text{ cm}^{-3}$ , while the BJT base is 560Å thick and doped to a level of  $5 \times 10^{17} \text{ cm}^{-3}$ . The emitter area in both cases was  $30 \times 30 \text{ um}^2$ . The HBT exhibits a peak current gain of approximately 400, and a gain of about 250 at a collector current of 1  $\mu$ A. This gain is achieved despite the fact that the base doping is 50 times greater than the emitter doping level of  $10^{17}/cm^3$ near the junction.



Fig.1 SIMS data for a 31% Ge HBT structure. The boron concentration in the base was calibrated by ion implanted SIMS standards in  $Si_{1-x}Ge_x$ . The emitter and collector profiles apply to all devices in thi study. The inset shows the device structure.



Fig.2 Gummel plot for an HBT (solid curves), and a silicon BJT (dashed curves).

The  $Si_{1-x}Ge_x/Si$  valence band discontinuity,  $\Delta E_v$  was extracted by measuring the normalized collector saturation current as a function of temperature, given by

$$\frac{I_{c(BBT)}}{I_{c(BJT)}} = \frac{(N_B W_B / D_B)_{BJT}}{(N_B W_B / D_B)_{HBT}} \exp\left(\frac{\Delta E_v}{kT}\right) \quad (1)$$

Semilog plots of the measured normalized collector current versus inverse temperature exhibit highly linear behavior, indicating that the temperature dependence of the pre-exponential ratio in Eq. (1) is negligible in the measurement temperature range from -50 to +130°C. Value extracted for the valence band discontinuity,  $\Delta$ Ev, compare favorably to the calculations of People for strained Si<sub>1-x</sub>Ge<sub>x</sub> layers<sup>10</sup>. The effect of doping-induced bandgap narrowing, which may be important, is currently being investigated.

HBTs with small emitter geometries were also fabricated to make a preliminary assessment of the high frequency behavior of such devices. It is expected that a device with low base resistance and high  $f_T$  can be constructed from this technology, and that such devices will be of interest in a wide range of high speed, low noise integrated circuit applications. For the device fabricated, an  $f_T$  of approximately 30GHz was obtained. This preliminary result would seem to offer great promise for the future. In general, the work demonstrates that high quality heterojunction devices can be fabricated in LRP-grown material.

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