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Selective Ge CVD as a Via Hole Filling Method and Self-Aligned Impurity Diffusion Microsource in Si Processing

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Low-temperature LPCVD with high-purity reactive, carrier, and purge gases was used for the experiments. The Ge deposition was found to be perfectly Si/SiO_2-selective and Ge was used to fill up via holes. The fabricated structures were tested with respect to their resistivities as well as their gettering and diffusion source capabilities in Ge-contacted Si diodes. The results show compatibility with conventional Si technology and reveal new applications for Ge CVD in low-temperature ULSI processing.

1. Introduction

Recently much attention has been payed to germanium in silicon technology. Beside SiGe alloys [1-6] also structures of alternating Si/Ge films [7] were investigated. Using several monolayers of germanium, superlattices and superstructures were formed, in which the bandgap can be tailored not only through the number of Ge atoms incorporated, but also through the amount of stress introduced into the lattice [8]. So far mainly molecular beam epitaxy (MBE) has been employed and remarkable progress has been achieved recently [9,10]. In this work, however, chemical vapor deposition (CVD) was used. CVD has some advantages like higher throughput, in situ doping and selective deposition [11]. In order to clarify the more complex chemical vapor deposition process of SiGe alloys, initiating low pressure CVD (LPCVD) experiments of pure Ge were done. The applicability of Ge CVD in Si processing was checked by selectively filling via holes with Ge and testing the parameters of Ge-contacted p-n diodes as well as the corresponding Ge/Si contact resistivities.

2. Experiment

An ultra high vacuum (UHV) compatible LPCVD reactor (base pressure 10^{-6} Pa) was used for the experiments. A schematic of the batch system consisting of a high-purity-nitrogen-purged transfer chamber connected to a resistance heated, horizontal hot wall furnace is shown in Fig. 1. Details are given elsewhere [12].

In the reactor epitaxial Ge films could be formed on silicon. To achieve epitaxial Ge deposition, temperatures between 350 °C and 400 °C were applied. The total pressure was kept in the range of 20 Pa,

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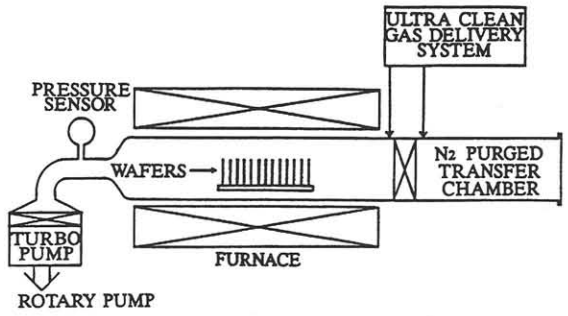

Fig. 1: The ultraclean hot wall LPCVD furnace which was used to deposit high-quality germanium and polysilicon.

while the GeH_4 partial pressure was 1 Pa to 10 Pa. Ultraclean processing was realized by using gases with moisture levels < 10 ppb in case of H_2, N_2, Si_2H_6 and PH_3, and < 23 ppb for GeH_4. The crystalline quality was checked by electron diffraction and scanning electron microscopy (SEM). The deposited thicknesses were measured by a Tencor Alpha Step.

In order to prepare the diode samples, boron-doped substrates (4-7 Ohm cm) with mirror-polished {100} surfaces were used. Schematics of the manufactured structures are shown in Fig. 2. After growing a thermal oxide the reverse sides were heavily boron-doped to achieve a better contact to the backside metallization. Then the samples were patterned. Before loading into the CVD reactor they were cleaned in several cycles in a 4:1 solution of high-purity H_2SO_4:H_2O_2, DI water, and 1% HF. Either Ge plus in-situ poly-Si (Fig. 2a) or, for comparison, only poly-Si (Fig. 2b) were deposited afterwards. The poly-Si was in-situ phosphorous-doped and formed at 600 °C out of a mixture of Si_2H_6, H_2 and PH_3 with a growth rate of about 5 nm/min. Poly-Si was necessary on top of the germanium to ensure a reliable contact to the evaporated aluminum metallization which was used on both sides of the wafers. Before aluminum deposition the samples were treated for 1 hour at temperatures up to 800 °C, after Al evaporation the wafers were tempered at 350 °C for 30 min.

Kelvin structures were utilized in order to determine the corresponding contact resistivities. As shown in Fig. 3, the samples were prepared in a similar way as described above. In addition a heavily phosphorous-doped region was formed in the substrates to make resistivity measurements possible. No backside metallization was necessary for this test. Again poly-Si structures without Ge were produced for comparison (Fig. 3b).

3. Results and Discussion

Since the deposited layers were about 500 nm thick, the crystallinity of the Ge films was not as good as for Si epitaxy [12]. In the employed region the discrepancies in

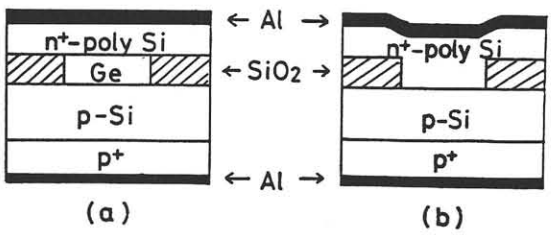

Fig. 2: The cross section of the diode structures produced for the tests. a.) The Ge-contacted diode and b.) the diode produced with poly-Si for reference.

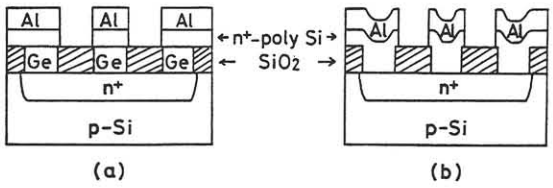

Fig. 3: Schematics of the Kelvin structures which were used to determine the Ge/Si contact resitivities. a.) The via holes filled selectively with Ge. b.) The poly-Si/Si contacts for comparison.

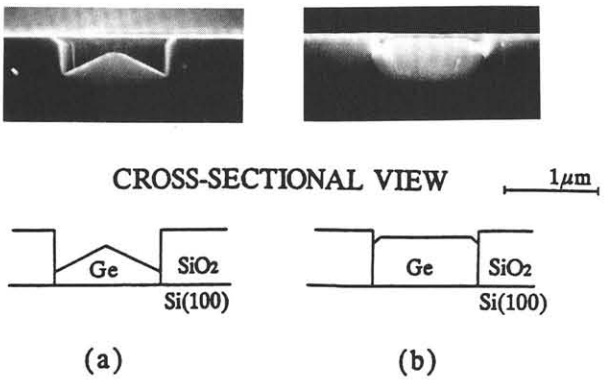

Fig. 4: SEM cross sections of selectively filled contact holes. a.) Epitaxial facet growth at a GeH_4 partial pressure of 1 Pa. b.) At 10 Pa GeH_4 partial pressure the contact can be filled up uniformly.

the lattice constants and thermal expansion coefficients between Si and Ge allow no strained layer growth [4,7] with low defect densities [3,5]. Fig. 4 shows examples for selectively filled contact holes. For GeH_4 partial pressures around 1 Pa (Fig. 4a) facet growth occurs [11]. At a partial pressure of 10 Pa via holes can be filled up uniformly (Fig. 4b). The deposition rate was about 2 nm/min at the employed temperatures. As can be seen in Fig. 2, no initial doping was used to form the p-n junctions. However, it was not the intention of this work to build heterodevices with the junctions at the Ge/Si interfaces. The idea is rather taking advantage of the gettering capabilities of germanium [13] to remove impurities from the junction regions and at the same time using the Ge plugs as diffusion microsources for forming shallow junctions in the Si substrate at low temperatures. Fig. 5 shows the forward and backward current densities of n^+-p diodes with (solid lines) and without Ge plugs (dashed lines) which were annealed at 800 °C. While the reverse currents are comparable, the slope in the forward current is a little steeper in case of the Ge-contacted diodes and the diode ideality factor is improved. Here it must be pointed out that, for easier producibility, the diodes in this experiment had rather large areas of $1.75*10^{-3}$ cm^2. In smaller devices a non-uniformity in the distribution of the dopants caused by grain boundary diffusion in the poly-Si should lead

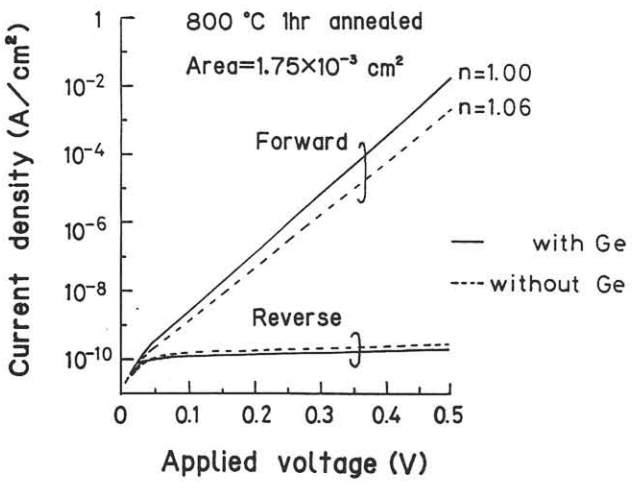

Fig. 5: Forward and backward current densities of n^+-p diodes with Ge plug (solid lines) and with poly-Si contact only (dashed lines). The diode ideality factors are 1.00 and 1.06, respectively.

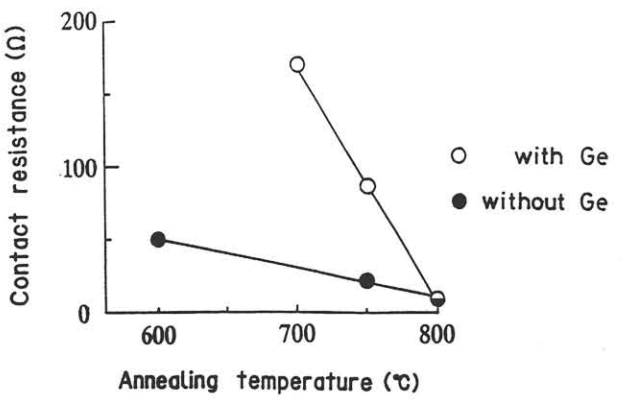

Fig. 6: The corresponding contact resistivities determined with the Kelvin structures after annealing and drive-in temperatures of 600, 700, 750 and 800 C. The contacting areas were about 20 square microns big. Open circles: Ge contacts, filled circles: poly-Si references.

to deviating results while a Ge-plug is able to produce more uniform dopant distributions, because the impurity diffusion coefficients are bigger in Ge than in Si [14].

The result for the contact resistivities is plotted in Fig. 6. Since the Ge-plugs were initially undoped, a big reduction in the resitivities can be observed for increasing annealing temperatures whereas the improvement for the poly-Si reference contacts is comparably small. After annealing at 800 °C, however, the same resistivities can be achieved for Ge and poly-Si contacts.

4. Summary

In the experiments presented germanium was used firstly as contact material, secondly for gettering impurities to reduce the trap density, and finally as a diffusion microsource to form p-n junctions in the Si substrate. All this could be achieved within the same process steps. It was possible to form high quality, Ge-contacted p-n junctions. Furtheron it could be shown for the first time that Ge CVD is suitable to fill up via holes selectively while achieving contact resistivities comparable to poly-Si contacts. The processes are compatible with conventional Si technology while employing temperatures not higher than 800 °C.

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