Effect of Atomic-Order Substrate Surface Planarization and O₂ Partial Pressure Control during Growth on Crystalline Quality of Si/Sr_xBa_{1-x}O/Si(111) Structure

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Lattice-matched mixed oxide $(Sr_xBa_{1-x}0)$ layers are grown on Si(111) substrate under two step 0_2 pressure control after atomicorder substrate surface planarization. Ion channeling measurements reveal that 300 nm mixed oxide $(Sr_{0.32}Ba_{0.68}0)$ films of good quality (channeling yield equal to 3%) can be grown on Si(111) at 850°C. The top-Si layers containing 10^5-10^6 cm⁻² order dislocations and no stacking fault are grown on these mixed oxide layers by introducing 4 nm solid phase epitaxy layers.

Introduction

Epitaxial growth of crystalline oxide films on Si substrates has been studied extensively for the purpose of realizing high quality SOI structures as well as high T_c superconducting transistors and interconnections formed on Si substrates.¹⁾²⁾ We recently reported on a Si/lattice-matched mixed oxide $(Sr_XBa_{1-X}0)/Si(111)$ stacked structure.³⁾ However, for applications, such as an insulator in silicon based devices, the qualities of the Si/oxide interface and the top-Si layer are decisive in determining the electrical properties. In order to improve these qualities three points were investigated: Preparing an atomic-order flat surface on an Si substrate prior to oxide deposition, Suppression of Si substrate surface roughing by etching through a chemical reaction between Si and oxygen at the initial oxide growth stage, and Suppression of 0 vacancy generation in the oxide layers during growth at the high temperatures (830-850°C). The results of the above investigations are presented in this paper.

Experimental Procedure

Experiments were performed in a ultrahigh vacuum (UHV) chamber equipped with a three electron-beam gun deposition system and a variable leak valve connected to an oxygen gas line. The base pressure and the pressure during Si growth in the UHV chamber were $1X10^{-9}$ and $7X10^{-9}$ Torr, respectively.

The Si wafers were chemically cleaned and finally boiled in solutions of $HC1:H_2O_2:H_2O$ (1:1:4) to produce a protective thin surface oxide. Prior to growth, this oxide was removed in the UHV chamber by heating the substrate to 800°C under a Si beam irradiation of 2x10¹³ atoms/cm²sec.⁴⁾ Next. the substrate temperature was lowered to a Si growth temperature (700°C). Then, 150 nm thick Si buffer layers were grown by molecular beam epitaxy (MBE) with a 0.05 nm/sec growth rate. In this experiment, the substrate was preheated at 1000°C for 50 min to obtain an atomic-order flat surface on the Si substrate for the purpose of high quality mixed oxide/Si interface formation.

Intensity oscillations in reflection

high energy electron diffraction (RHEED) from Si surface during growth were used as a probe for monitoring surface flatness of the substrate.⁵⁾ Acceleration voltage of the RHEED gun was 15-20 KV and the incident electron beam was parallel to $[1\overline{10}]$ in direction of the Si(111) substrates.

After RHEED oscillation monitoring, 0_2 was introduced into the chamber to in the pressure region of 1×10^{-7} - 1×10^{-5} Torr. Then, the substrate was heated to a oxide growth temperature (780°C). Details of the Si/Sr_xBa_{1-x}O/Si(111) stacked structure formation are described elsewhere.³⁾ The top-Si layers were grown on Sr_xBa_{1-x}O/Si kept at 700-800°C by introducing a solid-phaseepitaxy (SPE) Si layer at the interface.

The crystalline quality of the mixed oxides and the top-Si layers was examined by Rutherford backscattering/channeling (RBS/C) spectrometry. The crystallinity of the top-Si films was also investigated by the Sirtl etching method.

Results and Discussions

Figure 1 shows the intensity oscillation of a spot in a Si(111)-7X7 RHEED



Fig.1 RHEED intensity oscillations observed along the $[1\overline{1}0]$ azimuth of the Si(111) substrate during Si-MBE at 550 °C after a preheating of 1000 °C for 50 min.

pattern along the [110] azimuth during Si-MBE at 550°C after a pre-heating of 1000C for 50 min. The oscillations of the biatomic-layer mode is observed. These long lasting oscillations indicate that the atomic-order flat surface is realized after the preheating process.

The average dechanneling rate, $d\mathbf{x}/dz$, for 60 nm $\mathrm{Sr_xBa_{1-x}}$ O films is shown in Fig.2 as a function of O_2 pressure during the initial growth stage of the mixed oxide. The O_2 pressure was lowered to less than 5×10^{-7} Torr as soon as the Si substrate surface was fully covered with the mixed oxide layer. The boundary between 7X7 remained and 7X7 vanished region under O_2 pressures at 780°C, determined with RHEED, is also indicated. The oxide structural quality near the interface is effectively improved under 3.5×10^{-6} Torr O_2 pressure at 780°C as shown in this figure.



Fig.2 The average dechanneling rate, dx/dz, for 60 nm Sr_xBa_{1-x} 0 films as a function of 0_2 pressure during initial growth stage of mixed oxide. The boundary between 7X7 remained and 7X7 vanished region under 0_2 pressures at 780 °C, determined with RHEED, is also indicated.

The dependence of surface channeling yield (\mathbf{x}_0) and 0 composition on 0_2 pressure during growth for 60 nm mixed oxide films grown at 830°C is shown in Fig.3. The 0 vacancy generation in the epitaxial oxide



Fig.3 The dependence of surface channeling yield (x_0) and 0 composition on 0_2 pressure during growth for 60 nm mixed oxide films grown at 830 °C.

layer is suppressed by increasing 0_2 pressure. The composition of the oxide film is stoichiometric at $1X10^{-5}$ Torr. As a result, crystallinity is improved.

It was found from these investigations that the two step 0_2 pressure control is useful for single crystalline oxide quality improvement on Si substrate. The growth process (0_2 pressure-time) diagram is shown in Fig.4. In the following study, the mixed oxides were grown on Si(111) under the two step 0_2 pressure control after substrate surface atomic-order planarization process.



Fig.4 Time-0₂ pressure diagram of two step

growth process

The dependence of channeling yield on depth from the surface for 60 nm mixed oxide grown at (a) 780°C without 0_2 control (conventional growth condition),(b) 850°C under 0_2 control, and (c) 850°C under 0_2 control with substrate surface planarization, are compared in Fig.5. It can be seen from the figure that the mixed oxide structural quality is improved by the two step 0_2 pressure control and the substrate surface planarization process.



Fig.5 The dependence of channeling yield on depth from the surface for 60nm mixed oxide grown at (a) 780°C without O_2 control,(b) 850°C under O_2 control, and (c) 850°C under O_2 control with substrate surface planarization.

Figure 6 shows the channeling yield for $300 \text{ nm } \text{Sr}_{0.32}\text{Ba}_{0.68}0$ film grown at 850° C as a function of the depth from the surface. The data for the same thick mixed oxide film grown under conventional conditions is also shown in this figure. Comparing these profiles, the channeling yield (16%) for conventional film (a) is reduced to 10% at the interface. A surface channeling yield equal to 3% is obtained in the film (b) grown by the new process.

As the last step, the 500 nm top-Si layers were formed on the 300 nm $Sr_{0.32}Ba_{0.68}O/Si(111)$ structure by



Fig.6 The channeling yield for 300 nm $Sr_{0.32}Ba_{0.68}$ 0 grown at 850°C as a function of the depth from the surface. The data for the same thick mixed oxide film grown under conventional conditions is also shown for comparison.

introducing a 4 nm Si-SPE layer. To evaluate the type of crystal defects in the top-Si layer, the Sirtl etching method was used and the defects revealed by etching were observed through a SEM. The revealed defects were dislocations. No stacking fault was observed. In Fig.7, the depth profiles of the dislocation density in the top-Si layers grown on mixed oxides [(b) in Fig.6] is compared with that on mixed oxides [(a) in Fig.6] formed under conventional conditions. The solid line indicates a result for a homoepitaxial Si layer grown by introducing an SPE layer with the same thickness. The is reduced to 10^6 cm⁻² dislocation density the top-Si/mixed oxide interface. The near crystalline quality of the top-Si layers grown on the mixed oxide corresponding to (b) in Fig.6 is comparable to that of the homoepitaxial Si layers. The residual dislocation density of 10^6 cm⁻² at the interface is probably due to a defective SPE layer containing high density of micro twins. The density for homoepitaxial film without an SPE layer grown in our MBE apparatus is 10⁴.



Fig.7 The depth profiles of dislocation density in the top-Si layers grown on mixed oxides [(b) in Fig.6] is compared with that on mixed oxides [(a) in Fig.6] formed under conventoinal conditions. The dependence for the homoepitaxial Si layer grown by introducing an SPE layer with same thickness is plotted as the solid line.

Conclusion

(1) The substrate surface atomic-order planarization process improves the structural quality for the mixed oxide near the interface.

(2) The Si substrate roughing at the initial oxide growth stage and the 0 vacancy generation in the mixed oxide film during growth were suppressed by introducing a two step 0_2 pressure control process.

(3) In this experiment, 300 nm $Sr_{0.32}Ba_{0.68}0$ mixed oxide films of the best quality (χ_0 =3%) were grown on Si(111) at 850°C. The dislocation density in the top-Si layer grown on this mixed oxide was 10⁶ cm⁻² near the interface. No stacking fault was observed in this experiment.

Acknowledgment

The authors are grateful to Tetsushi Sakai for his continuous support. **Refferences** 1)K.Sawada,M.Ishida,T.Nakamura,and N.Ohtake:Appl.Phys.Lett.52(1988)1672. 2)M.Ihara,T.Kimura,H.Yamawaki,and K.Ikeda:IEEE Trans.MAG-25,No.2(1989)2470. 3)Y.Kado and Y.Arita:Ext.Abs.20th(1988) Inter.Conf.SSDM,C-1-2,p181-184. 4)M.Tabe:Jpn.J.Appl.Phys.21(1982)534. 5)T.Sakamoto,N.J.Kawai,T.Nakagawa,K.Ohta and T.Kojima:Surface Science,174(1986)651.