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High Voltage MOSFETs Using Submicron LSI Process

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High-voltage MOSFETs have been fabricated using a submicron LSI process. These MOSFETs have an offset drain region with a source field plate and a meshed-gate structure, and were designed by three-dimensional computer analysis. The MOSFETs were formed without any additional processing steps, since the offset drain region was formed simultaneously with the LDD of the low-voltage MOSFETs. As a result, an n-channel MOSFET with a 40-V breakdown voltage and a current density of above 200 A/cm^2 was achieved on the same chip as the submicron LSI devices.

1. Introduction

Recently, intelligent/smart power ICs (IPICs) have been developed for application to such electronic systems as used in automobiles or office automation equipment [1][2]. These ICs are expected to enable systems to achieve smaller size with higher reliability and lower cost. A higher density logic is therefore required on the same chip as the power devices to increase circuit functionality. Until recently, these ICs have been manufactured using a two or three micron rule process, but it is advantageous to fabricate them using a submicron LSI process for enhanced performance. However, high-voltage MOSFETs have not yet been realized on the same chip as submicron LSIs.

This paper describes the design and fabrication of high-voltage MOSFETs, suitable for the submicron LSI process. These devices are designed with a meshed-gate structure and a source field plate for high voltage and high current capability.

2. Submicron high-voltage MOSFETs

The relationship between breakdown voltages and design rules for high and low-voltage MOSFETs is shown in Fig. 1. As breakdown voltages decrease with the minimum size decreases, a lightly doped drain (LDD) structure is applied for the low-voltage devices. Breakdown voltages of higher than 10 V are obtained for 0.8-μm devices by using an LDD, but a high-voltage device has not yet been realized for the 1-μm process level. We applied an LDD to a high-voltage device, as an offset drain region with a field plate, to maintain a breakdown voltage of higher than 40 V and to achieve a high current handling capability.

Potential distributions for MOSFETs with and without a field plate are shown in Fig. 2. These were calculated using the three-dimensional device simulator CADDETH [3]. It shows that equipotential lines spread in the offset layer due to the source field plate. This means that electric field intensity of the proposed device will be reduced, compared to that of a conventional

device without a field plate. Some other devices of various offset lengths have also been calculated. As a result, a breakdown voltage of 40 V is obtained for a 4-μm offset length with a field plate. Based on this analysis, optimization of the proposed device structures, such as an offset drain region with a field plate, has been carried out. Additionally, the meshed-gate pattern is applied to increase device current and to reduce drain capacitance. As a result, the current handling capability and drain capacitance for the meshed-gate device increases by approximately 20 % and decreases by 40 %, respectively, in comparison to those of a conventional device with a striped-pattern.

The proposed cell structure for a high-voltage MOSFET has a 20-nm gate oxide, a 2-μm length channel and a 4-μm offset layer with a 30-μm size, as shown in Fig. 3. The field plate is constructed by an Al-source electrode.

3. Experiments and Discussion

A. Device Fabrication

Fabrication steps for high voltage MOSFETs are shown in Table 1. A conventional 0.8 μm CMOS process is modified to form the offset layer for the high-voltage MOSFETs at the same time as the LDD for the low-voltage devices, without any additional processing steps.

Table 1 Fabrication steps for high voltage MOSFETs.

(1) P-type wafer
(2) Well formation
(3) Local oxidation
(4) Gate formation
(5) LDD, offset layers formation
(6) Source, drain layers formation
(7) Metallization
(8) Passivation

B. Characteristics for high-voltage MOSFETs

Characteristics for a fabricated n-channel device that has an offset length of 4 μm and an ion dose of $5\times10^{12}/cm^2$ are shown in Fig. 4. A high transconductance of 100 mS (at V_{DS}=10 V, I_D=100 mA) and a specific on-resistance of 5 m$\Omega\cdot cm^2$ (at V_{DS}=1 V, V_{GS}=5 V) are realized, as shown in Fig. 4(a). Even with a gate driving voltage of 2 V, considerable current is obtained, suggesting the usefulness of this application to a low-voltage driver. Hard breakdown behavior, when a breakdown voltage of 41 V is obtained, is shown in Fig. 4(b).

Experimental results for breakdown voltages of the fabricated n-channel devices are shown in Fig. 5, as a parameter of offset length L_{off} and ion dose N_{DT}. Breakdown voltages of low voltage MOSFETs are also shown in the figure. Breakdown voltages for high-voltage MOSFETs change drastically depending on N_{DT}, while those of low-voltage MOSFETs are almost same. A maximum breakdown voltage of 47 V is achieved for an N_{DT} of $5\times10^{12}/cm^2$ in an optimized structure that has an offset layer and a source field plate. On the other hand, maximum breakdown voltage for a p-channel device was -25 V, because it was formed in the same n-well as the logic device. Simulation suggests that breakdown voltage for a p-channel device can be raised as high as that of n-channel, if n-well is optimized. The relationship between normalized current density and breakdown voltage for low-voltage and conventional high-voltage MOSFETs is shown in Fig. 6. Here, data for conventional 8-μm devices with a striped-gate pattern is measured by various devices such as those with a gate oxide of 100-130 nm thickness and offset drain regions with 5-40 μm lengths. It is pointed out that current densities for the proposed device are improved by about one decade compared to that for conventional ones. This is because channel widths were increased by the scaled-down cell structure

with a meshed-gate pattern.

C. Characteristics for low-voltage MOSFETs

Characteristics for the low-voltage and high-voltage devices of this process and the low-voltage device of a standard LSI process are shown in Table 2. As shown in the table, low-voltage device characteristics such as breakdown voltage, transconductance and CMOS ring oscillator delay scarcely change, showing little effect on the fabrication of high-voltage devices on the same chip.

D. CMOS driver switching characteristics

High-voltage CMOS drivers with breakdown voltages of above 20 V are fabricated. Channel width of the p-channel device is designed to be twice that of the n-channel one. Switching characteristics are measured with a load current of 200 mA, where the load has a 0.33-μH inductance and a 100-Ω resistance in series. A rise time of 16 ns and a fall time of 9.4 ns are achieved. These values are better than those for bipolar transistors with the same breakdown voltage.

4. Conclusion

High-voltage MOSFETs using a submicron LSI process have been discussed. These MOSFETs have an offset drain region with a source field plate and a meshed-gate structure, and were optimized by three-dimensional computer analysis. The offset drain region was formed simultaneously with the LDD of the submicron low-voltage MOSFETs, without any additional processing steps. As a result, an n-channel device, having a breakdown voltage of above 40 V and a current density of above 200 A/cm^2, was achieved on the same chip as submicron LSI devices. Additionally, the high-voltage CMOS driver, which consists of n and p-channel devices, was fabricated and successfully tested with an inductance load.

Acknowledgments

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Reference

[1] R. S. Wrathall et al., "Integrated circuits for the control of high power," IEDM Technical Digest, pp. 408-411, Dec., 1983.

[2] S. Storti et al., "A 30A 30V DMOS Motor Controller and Driver," ISSCC 88, pp. 192-193, Feb., 1988.

[3] T. Toyabe et al., "Three-Dimensional Device Simulator CADDETH with highly Convergent Matrix Solution Algorithms", IEEE Trans. on Electron Devices, Vol. ED-32, No. 10, pp. 2038-2044, 1985.

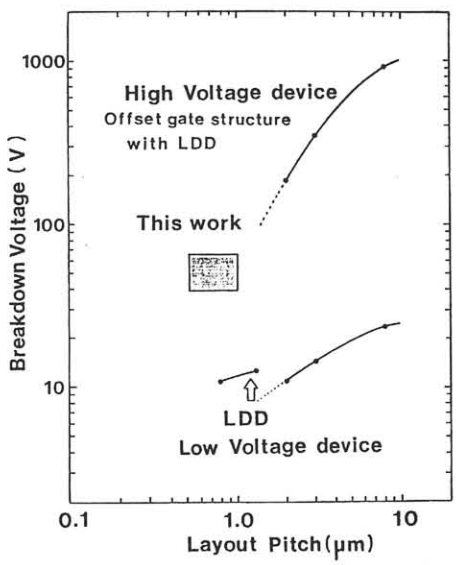
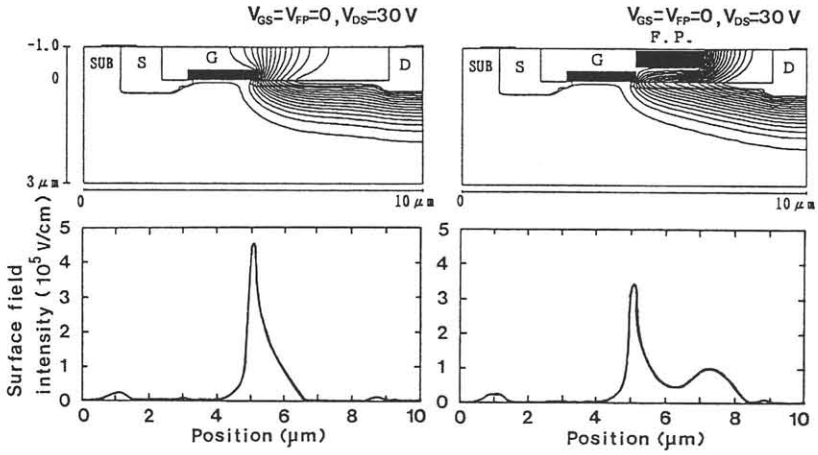


Fig. 1 The relationship between breakdown voltages and design rules for high and low-voltage MOSFETs.



(a) without a field plate. (b) with a field plate.

Fig. 2 Potential distributions for MOSFETs with and without a field plate.

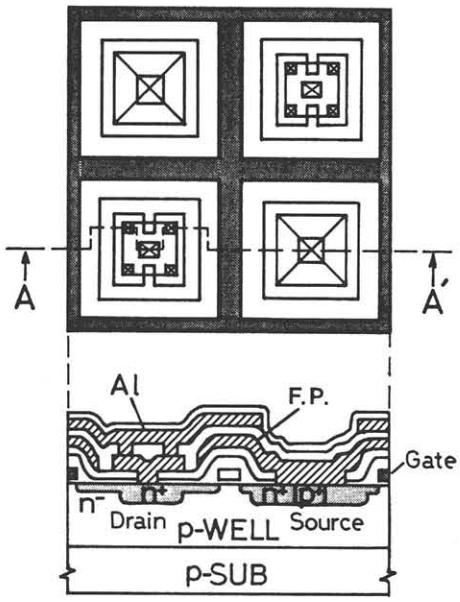
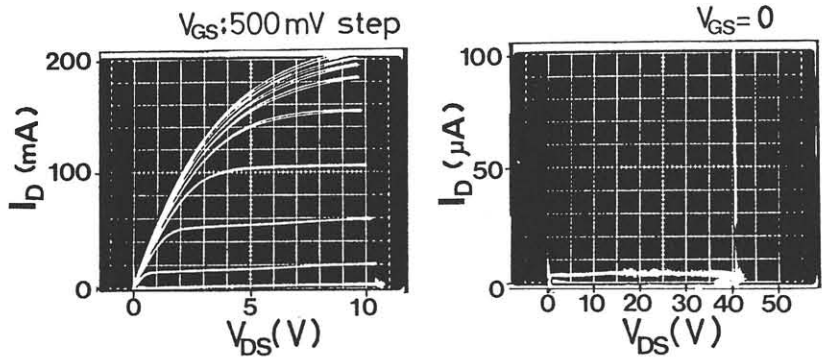


Fig. 3 The proposed cell structure for a high-voltage MOSFET.



(a) I-V characteristics. (b) Breakdown behavior.

Fig. 4 Characteristics for a fabricated n-channel device.

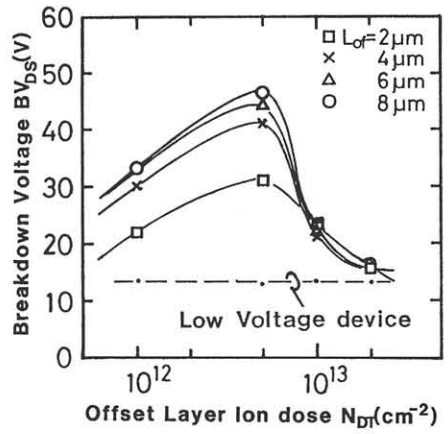


Fig. 5 Experimental results for breakdown voltages of the fabricated devices.

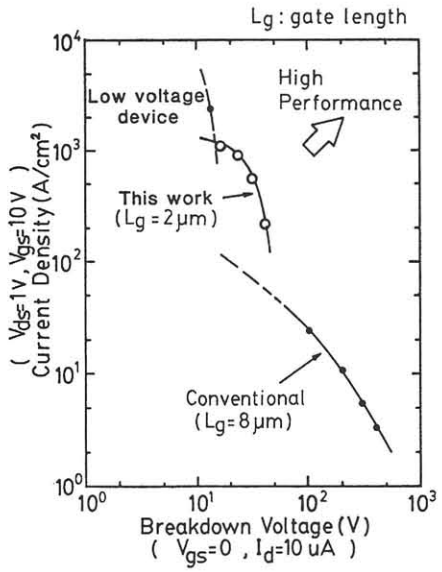


Fig. 6 Relationship between normalized current density and breakdown voltage.

Table 2 Characteristics for the low and high-voltage devices.

Process			Standard	Proposed	
Low Voltage MOSFET	N_{ch}	V_{th} (V)	0.7	0.6	V_{DS}=5V, I_D=10nA
		gm (mS)	1.1	1.0	V_{DS}=5V
		BV_{DS} (V)	13	13	V_{GS}=0, I_D=10nA
	P_{ch}	V_{th} (V)	−0.9	−0.9	V_{DS}=-5V, I_D=-10nA
		gm (mS)	0.6	0.6	V_{DS}=-5V
		BV_{DS} (V)	−15	−15	V_{GS}=0, I_D=-10nA
CMOS Ring OSC. Delay (ps/stage)			180	180	V_{DS}=5V
High Voltage MOSFET	N_{ch}	V_{th} (V)	−	0.4	V_{DS}=5V, I_D=10μA
		gm (mS)	−	100	V_{DS}=5V
		BV_{DS} (V)	−	40	V_{GS}=0, I_D=10μA
		R_{ON} (mΩ·cm²)	−	4.4	V_{DS}=10V, I_D=10mA
	P_{ch}	V_{th} (V)	−	−1.0	V_{DS}=-5V, I_D=-10μA
		gm (mS)	−	40	V_{DS}=-5V
		BV_{DS} (V)	−	−21	V_{GS}=0, I_D=-10μA
		R_{ON} (mΩ·cm²)	−	28	V_{DS}=-10V, I_D=-10mA