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A New Dielectric Isolation Technology Using Molten Silicon Spin Deposition

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A new polysilicon deposition technology using molten silicon has been developed. Using this technology, a 500μm thick polysilicon layer that acts as a mechanical support of DI substrate was deposited in only one minute. After the deposition of the polysilicon layer, the dislocation density in the substrate and the height of substrate curvature were $4 \times 10^{5}\ cm^{-2}$ and 200μm respectively and perfect filling of the polysilicon in the V-grooves was achieved. The application feasibility of this technology for LSI fabrication was confirmed by the performance of a 400V SLIC LSI.

1.Introduction

Dielectric isolation (DI) has many advantages, such as no latch-up actions, high voltage isolation, and high packing density. These advantages are especially attractive for high voltage LSIs. However, DI requires a thick polysilicon layer that acts as a mechanical support and a conventional CVD process using a hydrogen reduction of silicon halide takes too much time to deposit this layer. As a result, DI substrate is expensive and the applications of DI to LSIs have been limited.

We have developed a new polysilicon deposition technology using molten silicon to realize lower cost in forming the support layer. Using this technology, named MSSD (Molten Silicon Spin Deposition), a 500μm thick polysilicon layer was deposited at high speed and low cost. This paper presents this technology and the characteristics of a high voltage LSI fabricated using this technology.

2.Experimental

Fig.1 shows a schematic view of the setup in the present work. Basically, the setup consists of a silicon melting part and a spinning stage on which a silicon substrate is set. These parts are heated individually by graphite heaters in an argon ambient chamber. At first, high-purity polysilicon lumps are melted in a quartz

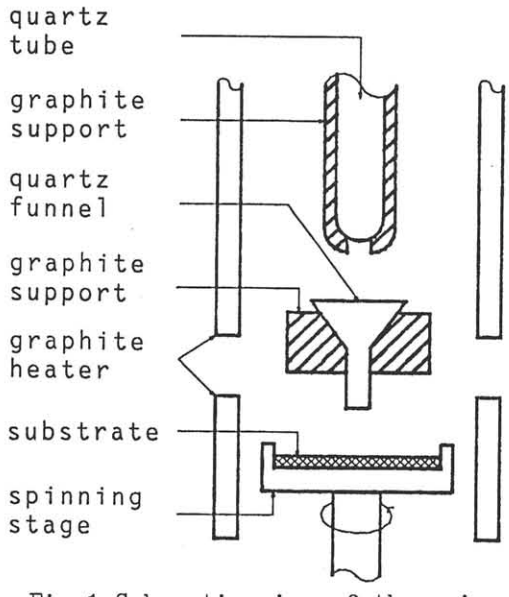


Fig.1 Schematic view of the main part of setup.

tube by heating it to 1440 °C. And 60-80g of molten silicon is dropped through a quartz funnel onto the heated spinning silicon substrate. The molten silicon which comes down at the center of the substrate is spread by centrifugal force and solidified. As a result, a 500-600μm thick polysilicon layer is deposited in only one minute. When the molten silicon is dropped, the rotating speed of the spinning stage is 60-80rpm and after the molten silicon is spread, it is raised to 300rpm. The thickness of the polysilicon layer is controlled by the duration of the 60-80rpm rotation.

The important points for application of MSSD to DI are to deposit a polysilicon layer on the substrate uniformly, to reduce dislocations induced in the substrate and curvature of the substrate, and to fill the polysilicon in V-grooves without any voids. In order to realize these three points, the layers that facilitate wetting with the molten silicon, the effect of the substrate temperature, and the effect of the atmospheric pressure were examined. In these experiments, the molten silicon temperature was set at 1440 °C and 4" diameter n-type (100) silicon wafers were used as substrates. The dislocations were observed using Wright etchant. In addition, to study MSSD application feasibility, a 400V LSI was fabricated.

3.Results and Discussions

The conditions of deposited polysilicon were examined for the substrates that had a SiO_2 layer, a Si_3N_4 layer on top of a SiO_2 layer, and a poly Si layer on top of a SiO_2 layer, on its surface respectively. When the molten silicon was dropped on a 1.5μm thick SiO_2 layer, the molten silicon didn't adhere to the substrate. The reason for this is that because the molten silicon has a relatively large contact angle with SiO_2[1]. overall wetting is prevented. When the molten silicon was dropped on a 0.2μm thick Si_3N_4 layer formed on top of the SiO_2 layer, the smaller contact angle[1] enabled the polysilicon to be well deposited at the perimeter of the substrate, but at the center where the molten silicon was dropped, the Si_3N_4 layer was peeled off and the molten silicon didn't adhere to this portion. When the molten silicon was dropped on a 30μm thick polysilicon layer formed by the CVD process on top of the SiO_2 layer, uniform deposition shown in Fig.2 was obtained. Fig.3 shows a typical grain structure of the polysilicon. Its grain size was a few hundred μm.

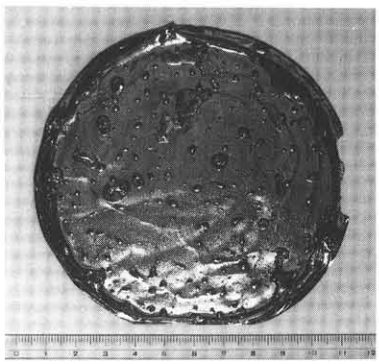


Fig.2 Polysilicon-deposited substrate.

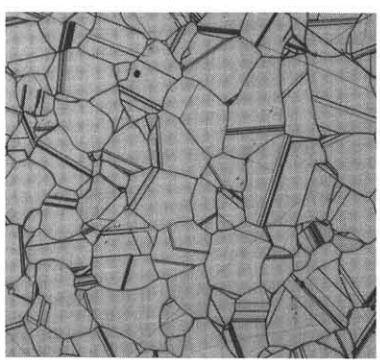


Fig.3 Typical grain structure of polysilicon.

The effect of the substrate temperature on the dislocation density and the curvature was examined in the range of 1225-1325 °C.

Fig.4 shows the result and Fig.5 shows photomicrographs of the dislocations induced in the substrate at 1225 °C and 1300 °C. At 1300°C the dislocation density is reduced to $4x10^5 cm^{-2}$ and the curvature height to 200μm. These values are sufficient for LSI fabrication. In Fig.4 the dislocation density decreases with increasing temperature. This shows that the cause of the dislocation generation is the thermal stress induced by the temperature gradient in the substrate at the moment the molten silicon is dropped. In Fig.4 the curvature height also decreases with increasing temperature. This shows that the cause of the curving is also the thermal stress. When the molten silicon is dropped, the upper side of the substrate becomes hotter and expands, therefore the substrate curves convexly toward the polysilicon layer side.

The effect of the atmospheric pressure on the filling of V-grooves was examined in the range of 10-760Torr. Fig.6 shows the dependence of the ratio of the number of filled V-grooves to the number of total V-grooves on pressure and Fig.7 shows the filling conditions of the polysilicon at 760Torr and 10Torr. While large voids in the V-grooves and small voids at the interface between polysilicon layers are observed at 760Torr, good filling of polysilicon is achieved at 10Torr. This shows that by reducing pressure, the residual Ar gas on the surface that causes the voids is easily removed and good filling is achieved.

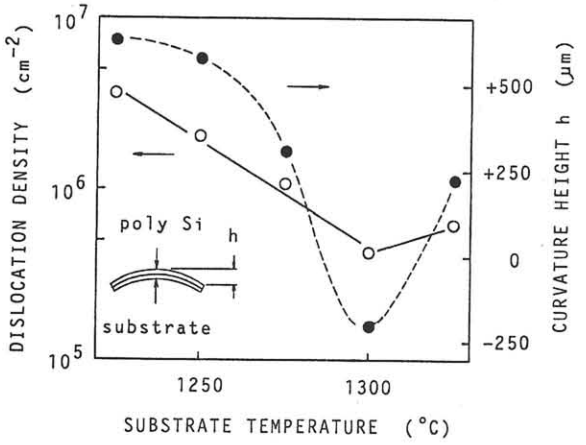
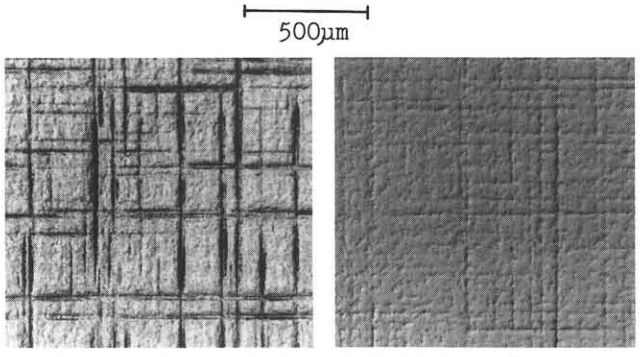


Fig.4 Dependence of dislocation density and curvature height on substrate temperature. The dislocation densities were examined in the center of the side opposite to the polysilicon layer.



(a) 1225°C (b) 1300°C

Fig.5 Photomicrographs of the dislocations induced in substrates.

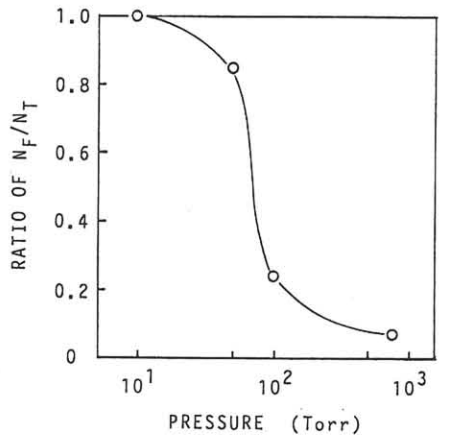
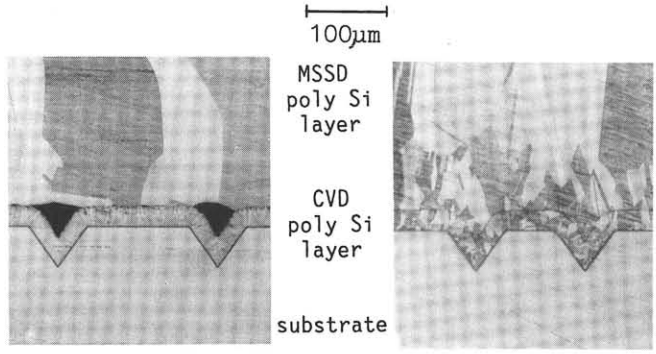


Fig.6 Dependence of the ratio of the number of filled V-grooves (N_F) to the number of total V-grooves (N_T) on pressure.



(a) 760Torr (b) 10Torr

Fig.7 Cross-sectional photomicrographs at V-grooves.

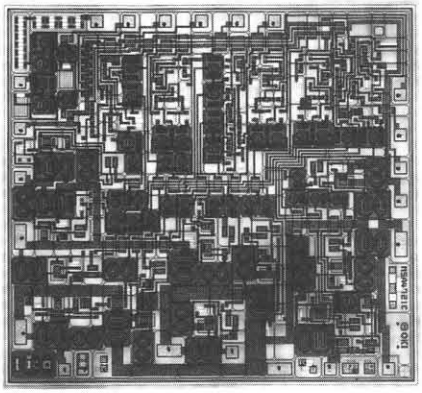
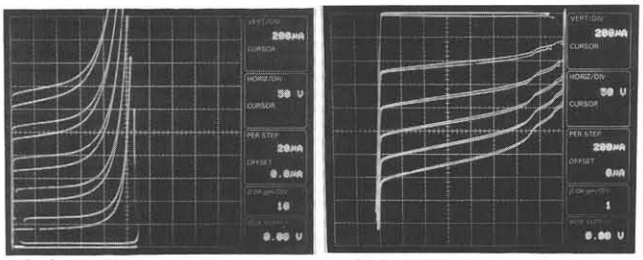


Fig.8 SLIC LSI chip photomicrograph.



(a) NPN transistor (b) PNP transistor

Fig.9 Typical I_C versus V_{CE} curves of high voltage transistors.

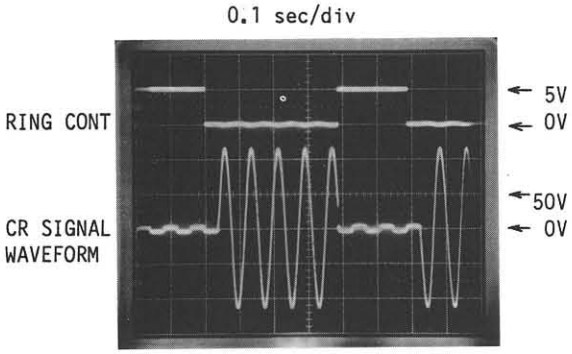


Fig.10 Ringing signal transmission waveforms.

Table:Electrical characteristics of high voltage SCR and low voltage transistors.

		Characteristics	MSSD	Conventional
High voltage SCR	NPN	h_{FE} (I_C=1mA,V_{CE}=5V)	10	10
		BV_{CEO} (I_C=1mA)	270V	270V
	PNP	h_{FE} (I_C=100uA,V_{CE}=5V)	1.2	1.5
		BV_{CEO} (I_C=100uA)	400V	400V
Low voltage transistor	NPN	h_{FE} (I_C=1mA,V_{CE}=5V)	100	100
	PNP	h_{FE} (I_C=100uA,V_{CE}=5V)	60	80

A 400V SLIC LSI[2] has been fabricated in DI substrates that were obtained by MSSD, on the basis of the above results. Fig.8 shows a photomicrograph of the LSI. This LSI has the functions of ringing, normal/reverse switching of lines, and network testing for subscriber line interface circuits, and the LSI includes 11 SCRs as switching elements. Fig.9 shows typical I_C versus V_{CE} curves of NPN and lateral PNP transistors that constitute SCR, and some major characteristics are summarized in the table, compared with devices fabricated in conventional DI substrate. The characteristics that are comparable to those of the conventional devices were obtained. In this table, h_{FE}s of both high and low voltage PNP transistors are a little smaller. This is caused by a little higher dislocation density of the substrate. The isolation voltage between single crystal islands was obtained at more than 1000V. Fig.10 shows ringing signal transmission waveforms. These waveforms show ordinary performance of the LSI.

4.Conclusion

Using MSSD, a thick polysilicon layer that acts as a mechanical support of DI substrate was deposited at high speed and low cost. A 400V SLIC LSI fabricated using MSSD showed good characteristics.

From these results, it has been established that this new technology is most promising in fabricating LSIs using DI at lower cost.

References

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2) K.Kawarada, T.Hayashi, Y.Inabe, and H.Imagawa; ISSCC Dig.Tech.Papers(1982) 202.