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Fabrication of $Si/CoSi_2/Si$ Permeable Base Transistor Using Self-Aligned and Two Step Molecular Beam Epitaxy

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A permeable base transistor (PBT) was successfully fabricated using $Si/CoSi_2/Si$ double heteroepitaxy. Two-step MBE (i.e. low temperature MBE and successive high temperature MBE) was used to form the high quality $Si/CoSi_2/Si$ double heterostructure. In addition, a new patterning method of CoSi2 films was developed, which utilizes the difference in surface energies. As a result, a high mutual conductance (50 mS/mm) of the PBT was obtained.

1. Introduction

Over the past few years there has been considerable interest in introducing new heterostructures in Si transistors. This is because so-called metal base transistors (MBT) [1] and/or PBT [2], in which thin crystalline silicide films are embedded in the Si, are considered to be potentially very valuable for realizing the high-speed operation of Si LSIs. Vojak pointed out the possibility of high frequency (> 25 GHz) operations in Si PBT with submicron geometry [3]. Ishibashi [4] and F.Arnaud.d'Avitaya [5] realized the Si PBT using a $Si/CoSi_2/Si$ structure. However, some problems in the crystal growth originating from lattice mismatch between $CoSi_2$ and Si have remained. More specifically, pinholes are introduced in films during high temperature growth, and high density defects are formed in the films during low temperature growth [6]. In addition, fine patterning of $CoSi_2$, which is crucial for device fabrication, can not be easily obtained by conventional dry etching techniques. Consequently, in order to realize the high performance Si PBT, some improvements in the crystal growth are necessary.

In line with this, the present paper describes the recently developed two-step MBE growth technique for obtaining high quality $Si/CoSi_2/Si$ double heterostructures and a self-aligned MBE method for obtaining fine patterning of $CoSi_2$ films. In addition, the fabrication of high performance PBT is demonstrated.

2. Experiments

In the experiments, etched grooves with 0.5 μm to a few μm line and space were made in Si(111) substrate using conventional photolithography and dry etching techniques. These samples were then processed in an ultrahigh vacuum (UHV) chamber (base pressure < 2×10^{-11} torr). Prior to crystal growth, sample surfaces were cleaned by the Ishiszaka-Shiraki etching method [7]. $CoSi_2$ films were grown on Si substrate by codeposition of Co and Si. The ratio between the Co beam and Si beam were kept constant during growth. Next a Si overlayer was grown on the $CoSi_2$ surface in the same UHV chamber. Both growth rates of $CoSi_2$ and Si were about 0.1 nm/sec.

The crystallinity and interface structure of $CoSi_2$ and Si films were examined by reflection high energy electron diffraction (RHEED) and X-ray photoemission spectroscopy (XPS). Surface morphology and crystallinity were investigated using Nomarsky microscope, scanning electron microscope (SEM) and cross-sectional transmission electron microscope (TEM) techniques. In addition, the electrical quality of the $Si/CoSi_2/Si$ heterostructure was evaluated by measuring of Schottky diode characteristics and the PBT's characteristics.

3. Formation of $Si/CoSi_2/Si$ Double Heterostructure

In order to obtain a high quality $Si/CoSi_2/Si$ double heterostructure, to start with, single heteroepitaxial growth ($CoSi_2/Si$) was investigated. The influences of flux ratio between Co and Si beam (10 at% Co-rich ~ 10 at% Si-rich), growth temperature (300 ~ 700 °C) and growth film thickness (10 ~ 50 nm) on crystallinity and surface morphology were examined. Figure 1 shows the surface morphology of $CoSi_2$ surfaces obtained by Nomarsky micrographs as a function of growth temperature and beam intensity ratio at the film thickness of 50 nm. The RHEED observation revealed that all $CoSi_2$ films were single crystal. Pinhole-free $CoSi_2$ films without surface ripples were obtained at the growth temperatures of 300 °C and 400 °C. At the growth temperature of 400 °C, the films deposited under the non-stoichiometric condition had pinholes (a few percent Co-rich) and/or surface roughness (a few percent Si-rich). At the growth temperature of 500 °C, all films had pinholes. When the film thickness of $CoSi_2$ was decreased, the growth temperature, at which smooth surface can be obtained, increased. For example, in the case of a 10 nm thickness, surface ripples were not detected at the growth temperatures up to 500 °C. These phenomena suggest that surface migration and/or strain energy of $CoSi_2$ is the driving force for pinhole formation.

The second step for the formation of $Si/CoSi_2/Si$ double heterostructure is the Si overgrowth on a smooth $CoSi_2/Si$ substrate. In the experiments, Si films (20 nm) were grown at different substrate temperatures (300 ~ 500 °C). RHEED and XPS measurement confirmed that all Si films were grown epitaxially without any Co segregation. Nomarsky microscope observation, however, indicated the existence of surface ripples at a growth temperature of 500 °C. Smooth surface was obtained at a growth temperature lower than 500 °C, however, the Si overlayer includes structural disorders.

To solve this problem, two-step MBE growth was examined. In that growth, a very thin Si layer (~ 2 nm) was grown at low temperature (300 ~ 400 °C) to stabilize the surface atoms of $CoSi_2$. Then, growth of a thick Si layer was grown at higher temperature (600 °C) to obtain high quality Si layers.

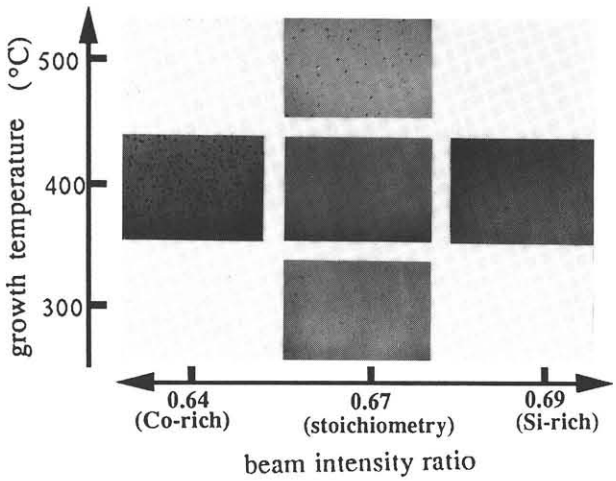

Fig.1 Influence of growth temperature and beam intensity ratio on surface morphology of $CoSi_2$.

The results of SEM and RHEED observations after two-step MBE, as shown in Fig.2, indicate that the surface morphology and crystallinity of the $Si/CoSi_2/Si$ heterostructure were very good. In addition, the XPS spectrum suggested that no surface segregation of Co had occurred during Si MBE. The atomic structure of the hetero-interfaces was examined by cross-sectional TEM. The lattice image of the cross-section, as shown in Fig.3, indicates that the upper and lower hetero interfaces between $CoSi_2$ and Si were atomically abrupt and smooth. In this way, a high quality $Si/CoSi_2/Si$ double heterostructure was realized using two-step MBE.

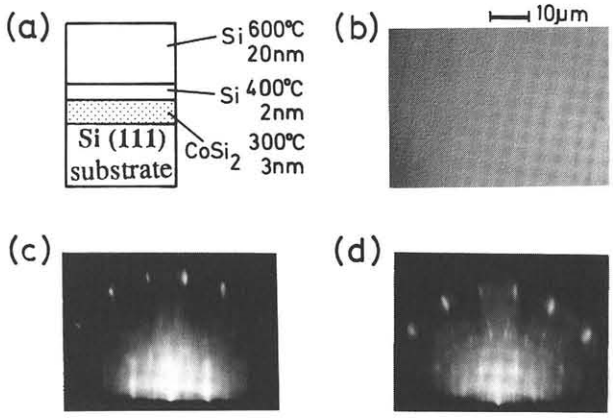

Fig.2 Schematic illustration and experimental results after two-step Si MBE growth. (a) sample structure, (b) surface morphology after Si growth at 400 °C, (c) RHEED pattern after Si growth at 400 °C and (d) RHEED pattern after Si growth at 600 °C.

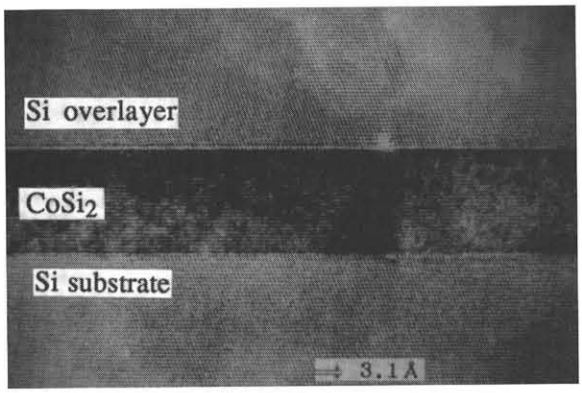

Fig.3 Cross-sectional lattice image of the Si/$CoSi_2$/Si double heterostructure observed by TEM.

4. Fine Patterning of $CoSi_2$ Electrode by Selective Growth

Experimental results in a previous section suggested that pinholes in $CoSi_2$ films are introduced to lower interface energy between $CoSi_2$ and Si [4]. In addition, it has been reported that the surface energy of Si(111) is smaller than that of Si(112) surface [8]. These results triggered the following idea: when the $CoSi_2$ film is grown on the etched grooves of a Si(111) surface, smooth $CoSi_2$ films are expected to grow on the top and the bottom (Si(111) surfaces), however, $CoSi_2$ deposited on the side walls (Si(112) surfaces) are thought to agglomerate to reduce interface energy.

To examine this idea, grooved patterns with different size of line and space (0.5 ~ 3 μm) were formed on a Si(111) substrate. Then $CoSi_2$ was grown at 300 ~ 600 °C under stoichiometric conditions. Electrical conductance measurement indicated that $CoSi_2$ films between the top and the bottom surfaces were electrically connected to each other when the growth temperature was lower than 300 °C. However, at growth temperatures higher than 400 °C, both two films were

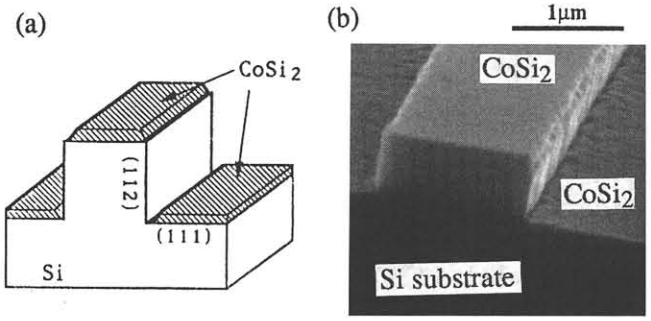

Fig.4 (a)Schematic illustration and (b)SEM micrograph after self-aligned $CoSi_2$ MBE growth on the etched grooves in Si substrate.

electrically isolated from each other. This result suggests that $CoSi_2$ films were grown selectively on the top and bottom surfaces of the etched grooves. Figure 4 shows a schematic illustration and the SEM image after self-aligned $CoSi_2$ MBE was grown on the etched grooves on a Si substrate. Thus, it was confirmed that the patterning of $CoSi_2$ films in the submicron range is established using this technique.

5. Fabrication of PBT

Using the newly developed techniques described in the previous sections, PBT were fabricated. In the fabrication, n-type Si ($n=10^{16}$ cm^{-3})/ n^+ type Si wafer were used as substrates. Here, the n^+ substrate was used as a drain of PBT. First, an n^+ Si source region was formed by P^+ ion implantation (50 keV, 1 x 10^{15} cm^{-2}) and annealing (900 °C, 5 min). Then, grooves of line and spacing 0.5 ~ 1.5 μm were formed on the Si surface by dry etching. MBE growth of $CoSi_2$ (10 nm thickness) was performed at the growth temperature of 500 °C. As a result, a $CoSi_2$ electrode was formed on the top and bottom Si surface of the etched grooves. These electrodes were buried in Si by the two-step Si MBE growth. A cross-sectional SEM image of the sample is shown in Fig.5, which clearly shows that the $CoSi_2$ electrode of submicron line and spacing were successfully embedded in Si. Finally, a Si overlayer was partially removed by dry etching to make contact holes for the gate and source electrodes.

Figure 6 shows the Schottky diode characteristics between source and gate. The diode factor of 1.15 was obtained under forward bias. Typical current-voltage

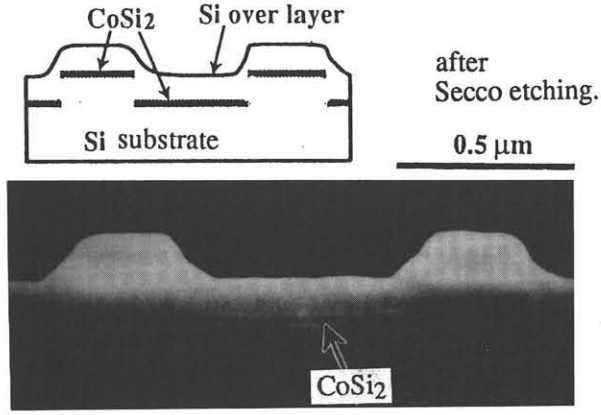

Fig.5 Cross-sectional SEM micrograph of buried $CoSi_2$ (10 nm thickness) electrodes after MBE. SEM

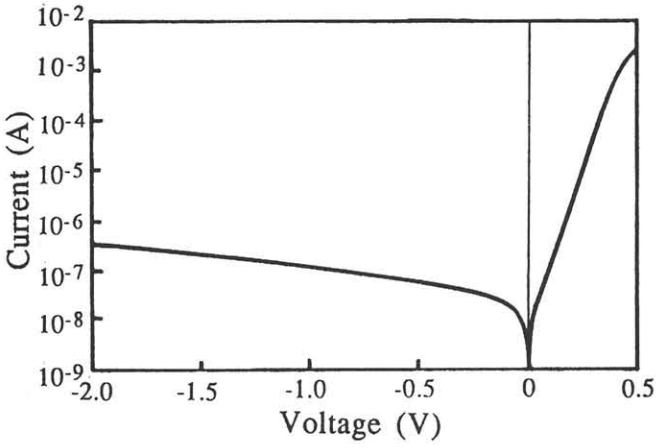

Fig.6 Schottky diode characteristics of $Si/CoSi_2$.

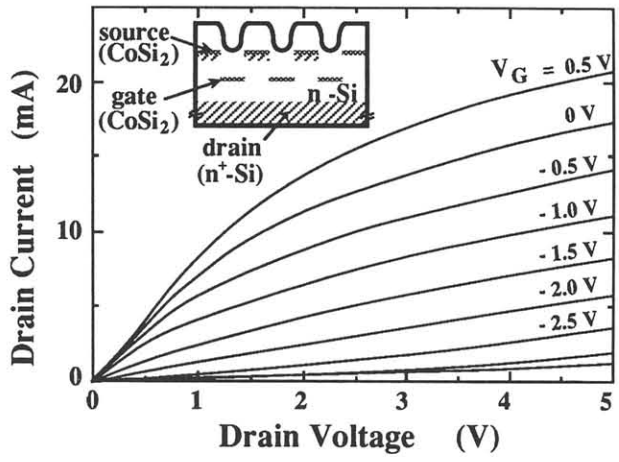

Fig.7 Typical current-voltage characteristics of PBT. Schematic illustration of PBT is also shown.

characteristics of PBT are shown in Fig.7. The mutual conductance (gm) of 50 mS/mm was obtained at the gate size ($CoSi_2$ line width) of 0.5 μm. This value of gm agrees well with the results of computer simulation, and is about ten times higher than that of previous works 4),5). These results suggest that the crystal quality at the interface between $CoSi_2$ and Si is quite good.

6. Summary

Formation of pinhole free and smooth $CoSi_2$ films with the lines and spacings from submicron to a few microns range were realized by a self-aligned MBE growth technique. In addition, high quality $Si/CoSi_2/Si$ double heterostructures were grown by a two-step Si MBE technique. As a result, fabrication of high performance PBT was demonstrated. These results indicate that the newly developed MBE techniques will prove to be powerful tools for building sophisticated Si devices, such as high performance PBT.

Acknowledgments

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