Extended Abstracts of the 21st Conference on Solid State Devices and Materials, Tokyo, 1989, pp. 89-92

A-5-4

Low Leakage SOIMOSFETs Fabricated Using a Wafer Bonding Method

M.Hashimoto, A.Ogasawara, M.Shimanoe, A.Nieda, H.Satoh, A.Yagi and T.Matsushita
Research & Development Div., Semiconductor Group
Sony Corp, 4-14-1 Atsugi, Kanagawa 243, Japan

A thin-film SOI substrate having a uniform thickness of 100±20nm realized by wafer bonding and selective polishing. CMOS transistors, which had low leakage current less than 0.1pA/μm, were fabricated on these substrates. It was observed that the source-drain breakdown voltage and the leakage current of n-channel transistors were improved with the LDD structure. It was concluded that these improvements depended upon lowering of the electric field at the drain.

1. INTRODUCTION

Recently thin film silicon-on-insulator (SOI) technologies have been taken notice of, because they offer unique advantages, especially in the field of CMOS applications. The absence of latch-up or the kink effect, low parastic capacitances, and radiation hardness are among the prime forces driving SOI research.[1),2)] However, when SOI technologies are put into practical use, there remain some problems such as high junction leakage current, or low source-drain breakdown voltage of n-channel transistors under low gate bias.[3)]

In this paper a newly developed method to fabricate SOI substrate is proposed. This method consists of a wafer bonding process and a selective polishing process, which should provide a high quality SOI substrate.[4)] Both n-channel transistors with LDD structures and p-channel transistors were fabricated on these substrates. The characteristics of them are described.

2.SUBSTRATE PREPARATION

The process flow of a SOI substrate is shown in Fig.1. A 5-inch (100) silicon wafer "A" was patterned with mesas, which correspond to device areas. A wafer of 30-50 ohm-cm resistivity was used for the control of the threshold voltage for p-channel transistors. The height of the mesas was about 0.1μm, which determined the SOI thickness after selective polishing. After 0.1μm thick thermal oxidization, a 1.0μm thick SiO_2 film and a 5.0μm thick polysilicon film were deposited (a). The polysilicon surface was polished into a flat mirror face (b), and wafer "A" was bonded with another silicon wafer "B" (c). The bonded wafers were annealed at 1,100°C so that the bonding was strengthened. After wafer "A" was thinned to several μm thick with a grinder (d), it was further thinned with a selective polishing method (e). In the selective polishing process the polishing rate of silicon decreases drastically once the oxide layer is exposed, and consequently thin film silicon islands

of uniform thickness can be left in the oxide layer. As shown in Fig.1(e) the isolation between device areas was completed when a SOI substrate was obtained.

A cross sectional SEM photograph of the SOI substrate fabricated with this method is shown in Fig.2. A silicon island floating in the underlying oxide was observed, which corresponds to device area.

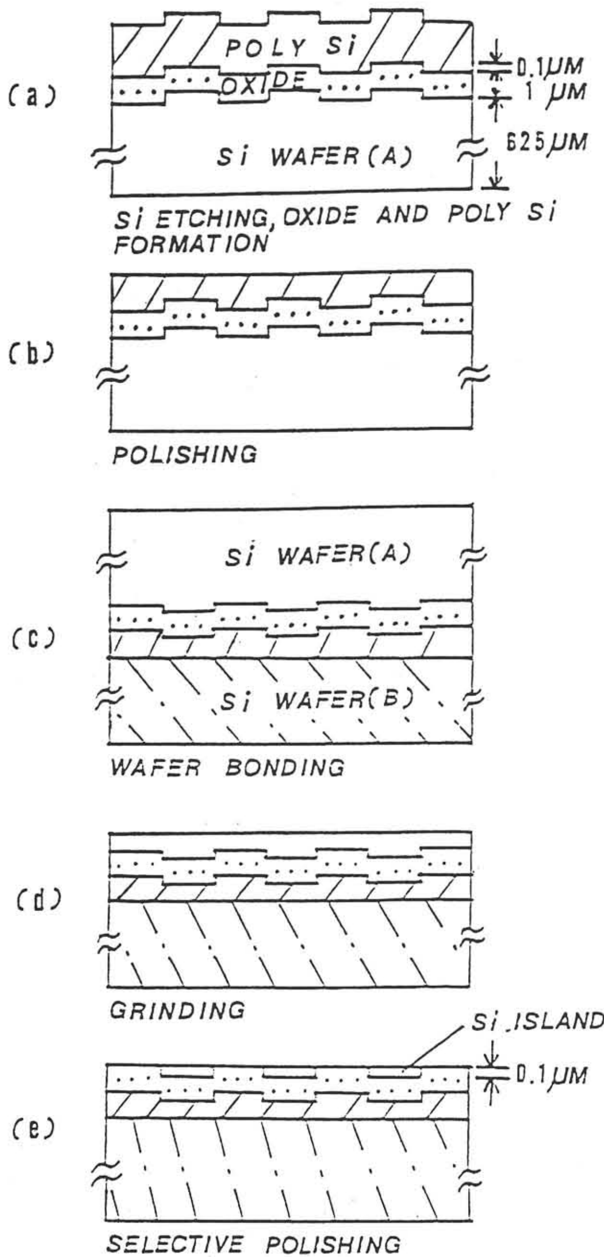

Fig.1 The process flow of a SOI substrate

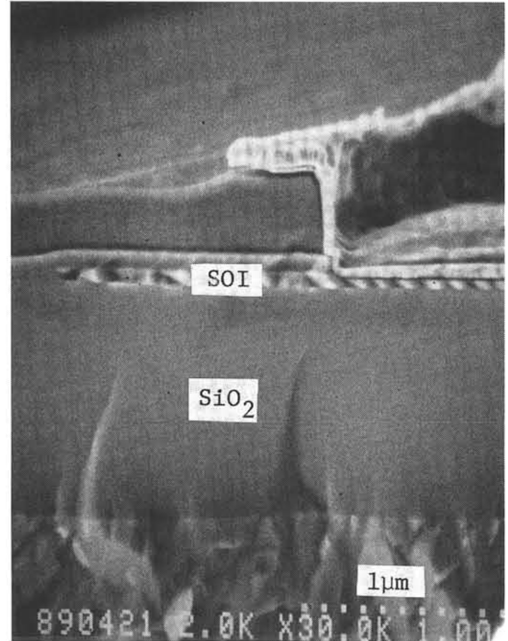

Fig.2 Cross sectional SEM photograph of the SOI substrate

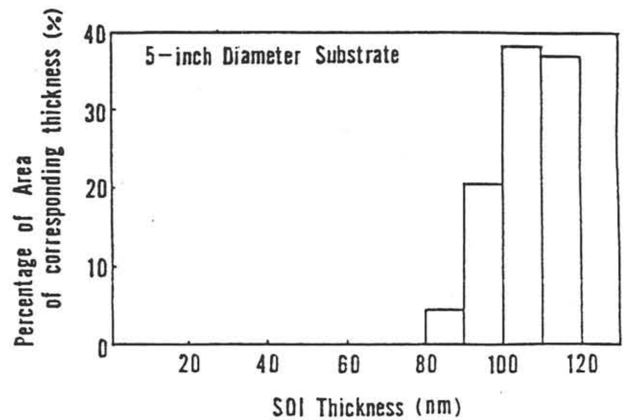

Fig.3 Typical variation of SOI thickness

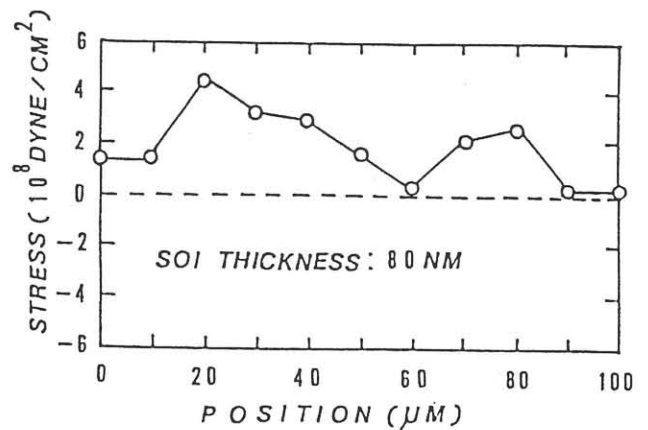

Fig.4 Residual stress in a 10,000μm^2 square Si island

Figure.3 shows the typical variation of SOI thickness. A uniformity of 100±20nm was obtained for a 5-inch substrate. Residual stress in a 100μm square silicon island was measured using Raman spectroscopy. Results of this measurement are shown in Fig.4. Tensile stress of $1\sim5\times10^{8}$ dyne/cm^{2} was obtained for a 80nm thick silicon island.

3. DEVICE FABRICATION PROCESS

CMOS transistors were fabricated in silicon islands on a 5-inch SOI substrate. There was no need for further isolation, because all isolation had been completed as mentioned previously. A 30nm thick gate oxide was formed at 900°C in wet ambient. BF_2 ions were implanted for the control of the threshold voltage in n-channel transistors. (No need for p-channel transistors. See Section 2.) A gate polysilicon film of 300nm thickness was deposited on the gate oxide and doped with phosphorus. A photolithgraphy process to form the gate electrode was carried out, and P ions were implanted to form a lightly -doped-drain (LDD) for n-channel transistors. After implantation of BF_2 to form the source and drain regions of p-channel transistors, side walls of oxide were formed using conventional methods. As ions were then implanted for n-channel transistors, and annealing was carried out at 940°C to activate the impurities. An Al electrode was used for electrical connections.

4. DEVICE CHARACTERISTICS AND DISCUSSION

Typical drain current vs gate voltage characteristics are shown in Fig.5, where W/L was 10μm/1μm for n-ch transistors and 10μm/1.2μm for p-ch transistors. The threshold voltage and subthreshold slope were 0.55V and 90mV/dec for n-ch

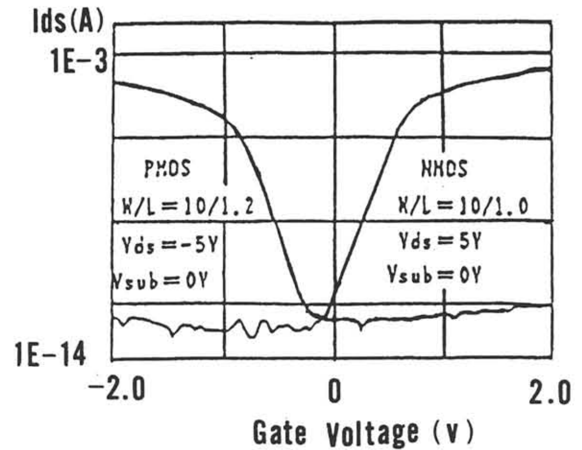

Fig.5 Id-Vg characteristics of SOIMOSFETs

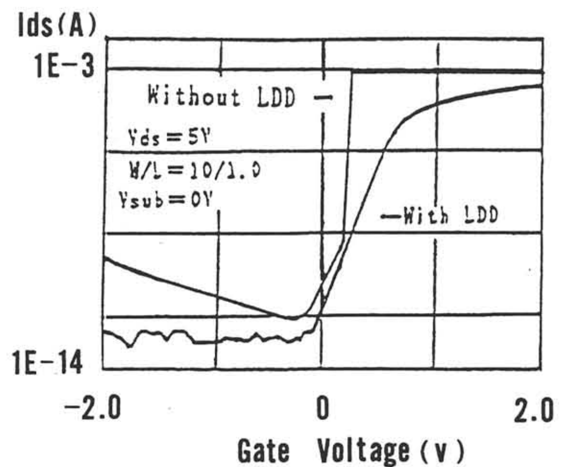

Fig.6 The comparison between the Id-Vg chracteristics of n-ch MOSFETs with and without LDD

MOSFETs, and -0.8V, 75mV/dec for p-ch MOSFETs respectivelly. The junction leakage currents for both transistors were less than 0.1pA/μm, comparing favoraly to bulk devices.

Low junction leakage currents could be achieved because devices were built on silicon islands surrounded by thermal oxide and n-ch MOSFETs had an LDD structure. Figure 6 shows the comparison between the Id-Vg characteristics of n-ch MOSFETs with and without LDD, for a drain voltage of 5V. The device without the LDD structure had exponentially increasing leakage current dependence on negative gate bias, which has been explained as tunneling current.[5] As shown in Fig.6 this leakage current could

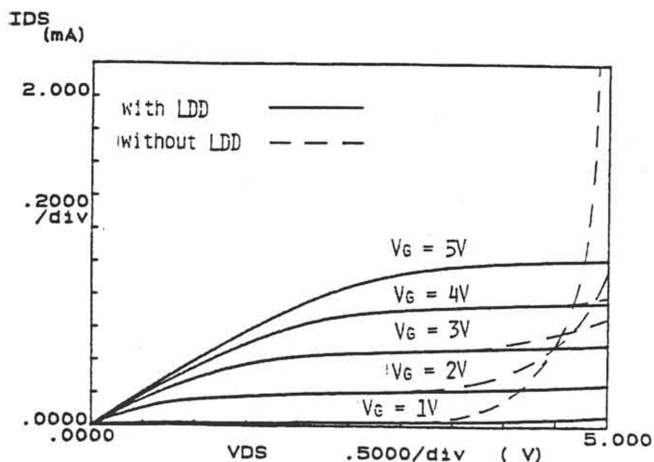

Fig.7 The comparison between the experimental results of the Id-Vg characteristics for an n-ch MOSFET with and without LDD

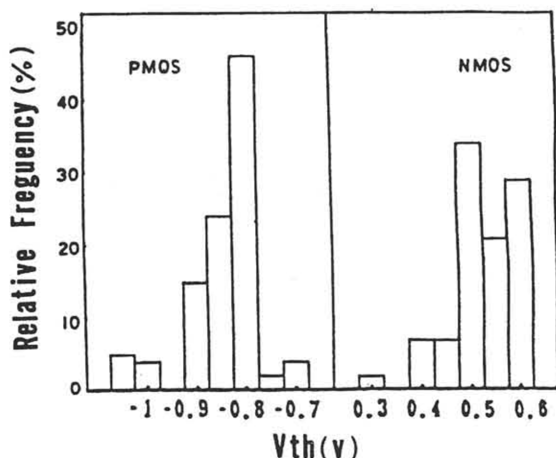

Fig.8 The variations of threshold voltage of SOI MOSFETs

be decreased with LDD structure. The remaining leakage current, which hardly depended on negative bias, was the generation current. It could be decreased by using a high quality SOI layer and enclosing the silicon islands with a thermal oxide. As for p-ch MOSFETs the leakage current was ruled by the generation current, so it could be decreased by the same method.

The source-drain breakdown voltage of n-ch MOSFETs was also improved with the LDD structure. A conventional n-ch SOIMOSFET without LDD exhibits abnormally high subthreshold slope, due to the low breakdown voltage under low gate bias. This phenomenon has been explained as the effect of impact ionization by the high electric field at the drain.[6),7)] Figure 6 shows that the high subthreshold slope disappeared due to lowering the electric field at the drain with the LDD structure. Figure 7 shows the comparison between the experimental results of the Id-Vd characteristics for an n-ch MOSFET with and without LDD. The improvement in source-drain breakdown voltage is observed.

The variations of threshold voltage were measured for n- and p-ch devices as shown in Fig.8 , where drain voltages were 5V and -5V respectively. For both types, the standard deviation of measured threshold voltage was about 0.08V.

5.CONCLUSION

A SOI substrate having a thickness of 100±20nm was realized by wafer bonding and selective polishing. CMOS transistors fabricated on these substrates had low junction leakage current and high source-drain breakdown voltage. Devices exhibited good uniformity in consideration of the variation of threshold voltage.

Acknowledgement

The authors express their gratitude to Y.Saitoh, S.Sakai, M.Matsuoka of Japan Silicon Co., T.Ohshima, M.Shinohara and H.Hayashi for their support.

Reference

1) J.P.Colinge: IEEE Circuits and Device Magazine (1987) 16.
2) J.P.Colinge: IEEE Electron Device Letters 9 (1988) No.2, 97.
3) M.Yoshimi et al.: Proc. Symp. VLSI technology, Kyoto (1989) p15.
4) T.Matsushita et al.: 47th Annual Device Research Conf. M.I.T(USA) VB-1 (1989)
5) J.Chen, T.Y.Chan: IEEE Electron Device Letters 8 (1987) No.11, 515.
6) J.P.Colinge: Microelectric Engineering 8 (1988) 127.
7) J.G.Fossum et al.: IEEE Electron Device Letters 8 (1987) No.11, 544.