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An 8 nm-thick Polysilicon MOS Transistor and Its Thin Film Effects

T. Hashimoto , T. Kobayashi , T. Mine , T. Yamanaka , N. Hashimoto
A. Shimizu* , T. Nishida and Y. Kawamoto

Central Research Laboratory, Hitachi Ltd., Kokubunji, Tokyo 185, JAPAN
*Hitachi VLSI Engineering Corp., Tokyo JAPAN

Submicron p-channel polysilicon MOS transistors have been fabricated in a ultra-thin polysilicon film. These devices show excellent characteristics due to thin film effects in off-current, subthreshold slope and punchthrough resistance. A key fabrication technology is the formation of continuous polysilicon film less than 10nm-thick.

In LPCVD silicon deposition the nucleus density on CVD SiO_2 is found to be higher than that on thermal SiO_2. An 8nm-thick continuous silicon film is formed on CVD SiO_2 for polysilicon MOS transistor.

INTRODUCTION

In recent years, there have been many reports on polysilicon MOS transistors (poly-Si MOS) for application to VLSI [1,2]. We have already reported a new type of memory cell with a poly-Si p-channel MOS load and a cross-coupled capacitor for high packing density SRAM [3]. This cell has many advantages, such as reduction in stand-by power, improvement of retention characteristics and soft error immunity. In order to achieve them, a high on/off current ratio is demanded for poly-Si pMOS load [4].

There have been several reports on increase of grain size more than 1 μm by recrystallization of Si films, which are amorphized by Si^+ ion implantation [5]. They have reported high on-current (I_{ON}) because of the film's high field mobility. Furthermore, the benefits of a thin poly-Si film have been proposed to accomplish low off-current (I_{OFF}). However, there is a limit to deposit a thin poly-Si film using a conventional LPCVD technique, because a Si film has an island structure in the initial stage of the deposition.

To overcome this problem, a new technology has been developed to obtain continuous Si film less than 10nm-thick. The device fabricated in this film showed not only low I_{OFF} but also excellent performances in other areas. In this report we describe the poly-Si deposition technology and the electrical characteristics of the poly-Si MOS transistor.

EXPERIMENTAL

1. Formation and observation of Si film

Si films were deposited on insulators on Si wafers in a conventional LPCVD reactor. The flow rate of SiH_4 as a source gas was fixed at 60sccm. Total pressure in the reactor was 106Pa and temperature was 515~630℃.

The surface morphology of the Si films was inspected by scanning electron microscopy (SEM). The uniformity and the thickness of the ultra-thin Si films were verified using transmission electron microscopy(TEM).

2. Device structure and fabrication

A schematic cross-section of the poly-Si pMOS is shown in Fig.1. It has so-called under-gate structure. A 100nm-thick poly-Si film was deposited at 620℃ by LPCVD on a

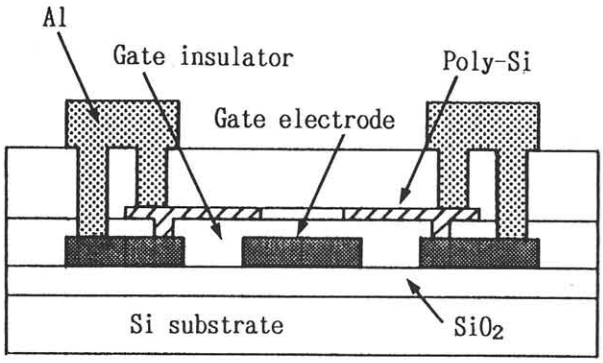

Fig.1 Schematic cross-section of the poly-Si p-channel MOSFET

100nm-thick thermally grown SiO_2. BF_2^+ ion implantation and RIE were carried out to form a gate electrode. Then a 22~36nm-thick gate oxide was deposited using a reaction of SiH_4 and N_2O at 800℃. An 8~38nm-thick Si film was deposited at 530℃. When device isolation was accomplished, BF_2^+ at a dose of $2E14cm^{-2}$ was implanted in the source/drain regions. After a 100nm-thick CVD SiO_2 and a 350nm-thick boro-phospho-silicate glass (BPSG) film were deposited as an inter-layer, annealing was carried out at 900℃ in N_2 for 30min. After contact hole delineation, an Al-Si film was deposited, patterned and sintered at 450℃ in H_2. A 500nm-thick PSG film or plasma-deposited Si_3N_4 film was then formed as encapsulation layer, hydrogen passivation was achieved by subsequent annealing at 450℃ in N_2.

RESULTS AND DISCUSSIONS

1. Formation of ultra-thin poly-Si film

Figure 2 shows SEM micrographs of Si films on thermal SiO_2 at different deposition times. In the initial stage we can find that the film has an island structure. The film thickness must be more than 30nm to form a continuous film in this condition. This phenomenon is explicable by the following deposition mechanism. In the initial stage nucleations occurred in small clusters on the insulator at a certain probability. As time progresses these nuclei grow and coalesce. Finally a continuous film is formed which then thickens.

According to this deposition mechanism, a thinner continuous film can be obtained by increasing the nucleus density. We think that nucleus density strongly depends on the substrate insulator. Thus we investigated the surface morphology in the initial stage of deposition on different insulators: thermal SiO_2, CVD SiO_2 and CVD Si_3N_4. Deposition temperature was 630℃. These results are shown in Fig.3. Obviously nucleus density on the CVD insulators is higher than that on thermal SiO_2. On thermal SiO_2, the film has an island structure and the height of each island being about 15nm. However, on the CVD SiO_2 or Si_3N_4, films of the same thickness are almost continuous. Furthermore, deposition temperature also influences nucleus density. We can obtain an 8nm-thick continuous film by decreasing the deposition temperature from 630℃ to 530℃. For poly-Si pMOS with an under-gate structure, the CVD insulator can be used as a gate insulator. The CVD SiO_2 film is chosen because of its good properties as a gate insulator.

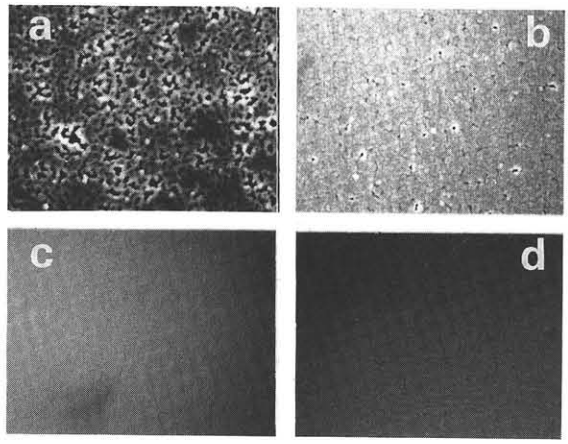

Fig.2 SEM micrographs of Si film surface at different deposition times
Films were deposited at 520℃ on thermal SiO_2.
a)20min b)30min c)40min d)60min

2. Device characteristics

Figure 4 shows subthreshold characteristics of poly-Si pMOS with several channel lengths for two different poly-Si thickness. Figure 5 shows I_{OFF} as a function of poly-Si thickness. I_{OFF} decreases with poly-Si thickness. I_{OFF} is considered as generation current at the

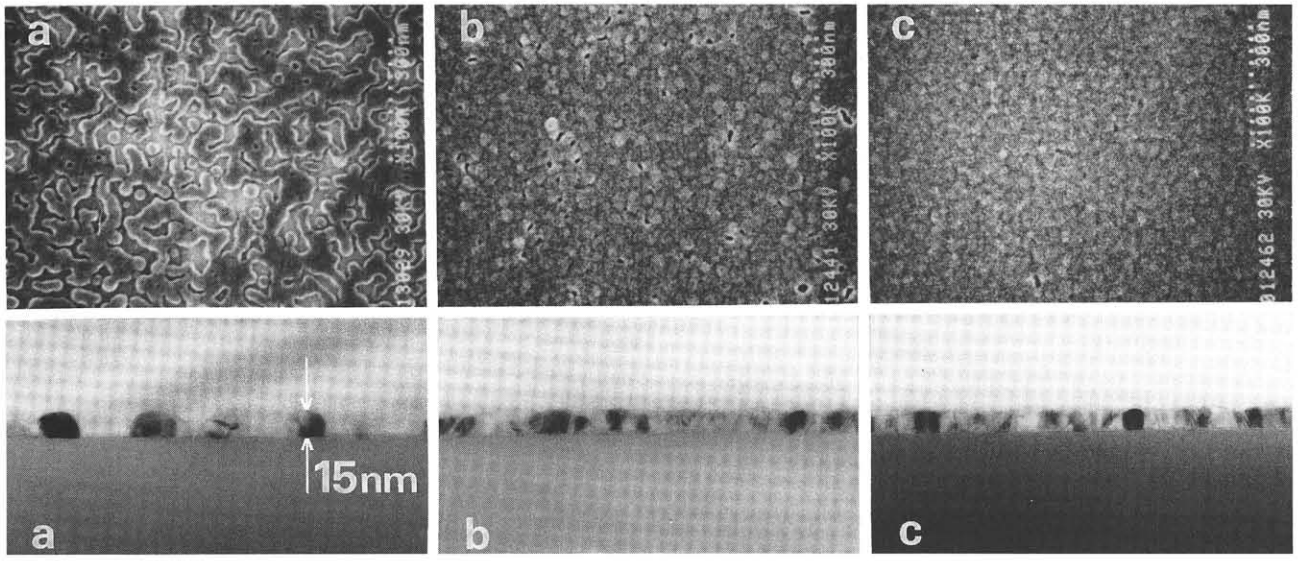

Fig. 3 SEM(upper) and TEM(lower) micrographs of Si films deposited on a)thermal SiO_2, b)CVD SiO_2, c)CVD Si_3N_4 Films were deposited at 630℃ for 2min.

drain p-n junction [6]. Junction area increases with poly-Si thickness. An 8nm-thick poly-Si pMOS has sufficiently small I_{OFF}. A typical I_{OFF} (at V_D=-3.5V, V_G=0V) is as low as 0.04pA shown in Fig. 4, which corresponds to 0.16 μA stand-by current for 4-Mbit SRAM.

Figure 6 shows subthreshold swing(S) as a function of poly-Si thickness. The decrease in S factor is very important, because I_{ON} is determined mainly by S factor. By thinning the poly-Si film from 38nm to 8nm, S factor is decreased from 0.54V / decade to 0.37V / decade without hydrogen passivation, which results in the increase of I_{ON} (at $V_D = V_G = -4V$) approximately five times. A similar improvement is observed in a single crystalline Si SOI MOSFET [7]. It is observed at about 100nm critical thickness, while about 10nm-thick is critical for a poly-Si MOS.

Figure 7 shows ΔV_{TH} as a function of channel length. Short channel effect is suppressed by reducing the poly-Si thickness. This result seems the same as the thin film effect in single Si SOI pointed out in ref. [8]. An 8nm-thick poly-Si pMOS do not show punchthrough even if channel length is 0.8 μm,

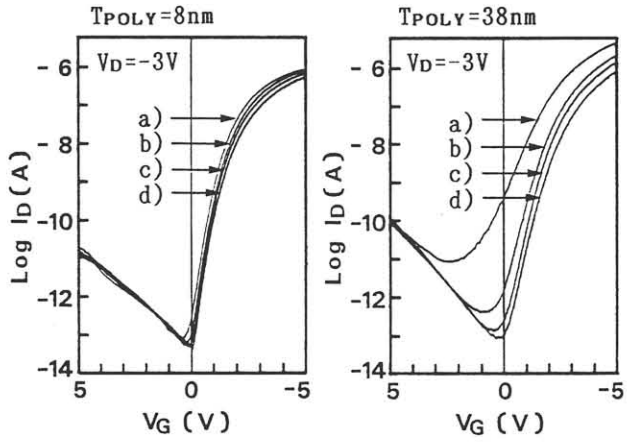

Fig. 4 Subthreshold characteristics of p-channel MOSFETs for different channel lengths a)0.8 μm, b)1.0 μm, c)1.2 μm, d)1.6 μm

while a 38nm-thick device shows increase of I_{OFF} due to punchthrough at the same condition. Therefore this ultra-thin Si film is quite attractive for future three-dimensional SRAM cells.

CONCLUSION

We have achieved a high performance poly-Si pMOS which has low Ioff, sharp subthreshold slope and high punchthrough

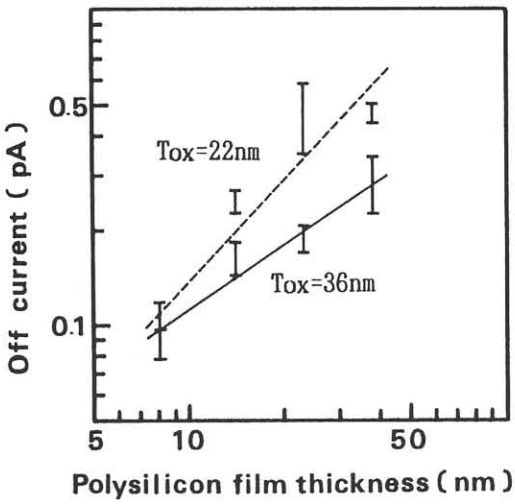

Fig.5 Off current vs. poly-Si film thickness L/W=1.6/0.6(μm), V_D=-3.5V

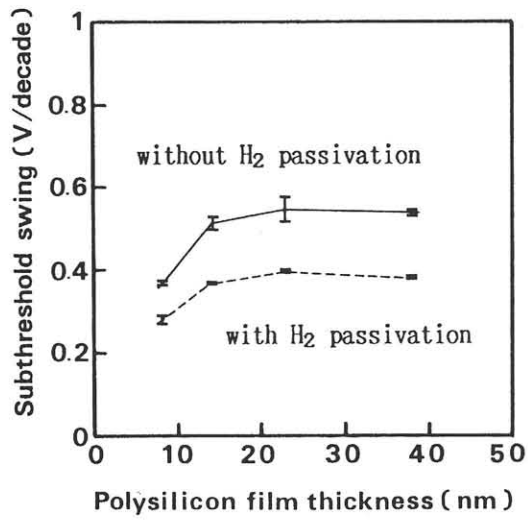

Fig.6 Subthreshold swing vs. poly-Si film thickness L/W=1.6/0.6(μm), V_D=-0.1V

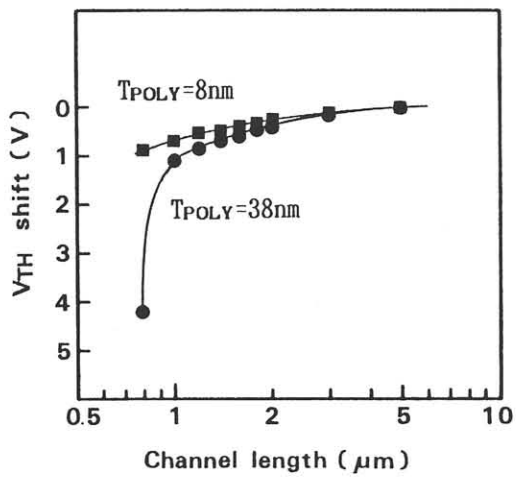

Fig.7 V_{TH} shift(ΔV_{TH}) dependence on channel length
$\Delta V_{TH}=V_{TH}(L=5\,\mu m)-V_{TH}(L=L)$

resistance by using an ultra-thin poly-Si film less than 10nm. This film is obtained by using CVD SiO_2 as a substrate insulator on which nucleus density is higher than that on thermal SiO_2.

Thus, the proposed poly-Si pMOS shows excellent performances and high potential for future high packing density SRAM cells using deep submicron technology.

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