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Three Dimentional Effects on Submicrometer Diagonal MOSFETs

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The "*three dimensional effects*" in submicron diagonal-layout MOSFETs, such as V_{th} shift suppression and hot currier reduction, are discussed. These effects are caused by a three-dimensional current path modulated by a diagonal layout. Such a three dimensional current path modulation reduces the high electric field at the drain and suppresses the short-channel effects such as V_{th} lowering. Also, this reduced electric field realizes small substrate current. Thus, diagonal-layout MOSFETs provide good device characteristics, as well as high packing density required for future ULSI's

Introduction

A new generation of MOS memories has been created every three years, and the capacities of successive generations have been four times that of the previous generation's. To achieve a high packing density, reduction of only the minimum device dimension is not sufficient. Thus, it is indispensable to devise a memory cell structure whose size can be minimized.

Under this situation, the "diagonal-layout MOSFETs" (D-L MOSFETs) whose active area is set diagonally across the gate electrode are expected to become general for DRAM's and SRAM's. For example, S. Kimura et al.[1] reported a new stacked capacitor cell for which a diagonally placed active area is essential.

Conventional MOSFETs are called "normal MOSFETs" in this paper to distinguish them from the "diagonal-layout MOSFETs ".

A typical layout of a D-L MOSFETs is shown as a inset in Fig. 1. The channel width W_D is defined as the width of gate width, which is measured perpendicular to gate, and the channel length L_D is defined as the width of the active area. Both W_D and L_D are defined as the length of photomask.

This paper presents the electrical characteristics of D-L MOSFETs. The distinctive features of D-L MOSFETs are interpreted on the basis of geometrical effects.

Current Path Modulation

The electrical characteristics of diagonal-layout MOSFETs are found to be strongly affected by the current path.

The channel width dependence on the transconductance in D-L MOSFETs and in normal MOSFETs are shown in Fig. 1. The transconductance in D-L MOSFETs dose not exhibit simple device dimension dependence; $G_m \propto W / L$. Here, W is the effective channel width and L is the effective channel length.

This complicated behavior of transconductance in D-L MOSFETs originated from current path modulations. The three-dimensional device simulator (CADDETH [2]) was employed to analyze the current path in D-L MOSFETs, and the results are shown in Fig. 2.

To comprehend the current path modulation in D-L MOSFETs, we first consider two extreme cases. One is where D-L MOSFET's width is large compared with its channel length (W » L). The other extreme is where its channel width is small compared with its channel length (W « L).

In the former case, current flows perpendicular to the gate electrode, as shown in Fig. 2 (a). This is because current tends to take the shortest path between source and drain. The virtual channel width which is measured perpendicular to the current path becomes $\sqrt{2}$ W_D. This effect is called "*channel widening effect*". In the latter case, current flows along the active area, as shown in Fig. 2 (c). The virtual channel length which is defined as a length measured along the current path becomes $\sqrt{2}$ L_D. The virtual channel width remains W_D. This effect is hereafter called "*channel lengthening effect*".

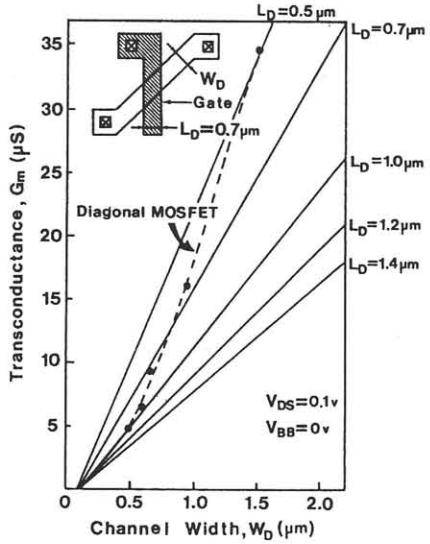

Fig. 1 Transconductance in Diagonal-layout MOSFETs as a function of channel width. Typical layout of a diagonal-layout MOSFET is shown as an inset.

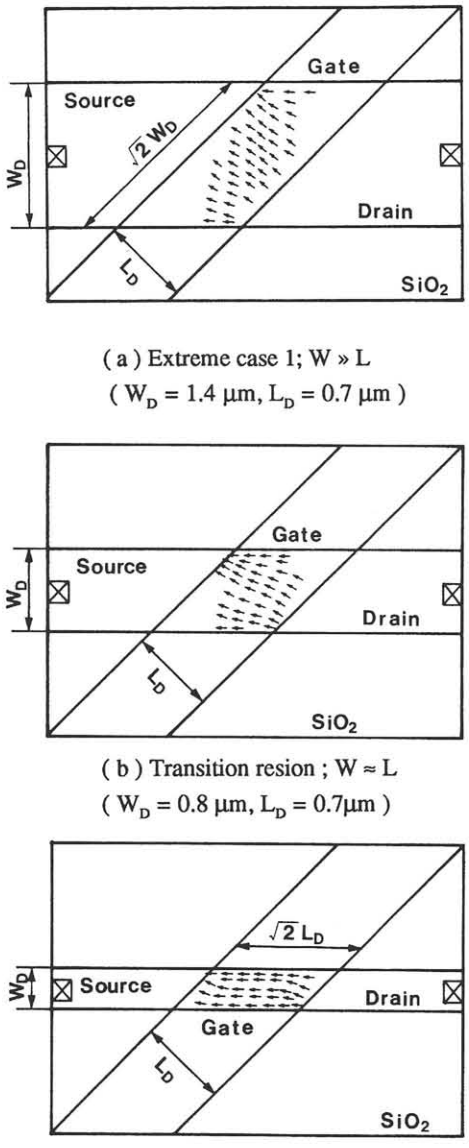

Fig. 2 Current path in diagonal-layout MOSFETs. Culculations were made under the bias conditions; V_{DS} = 0.1V, V_{BB} = 0V, and V_G = 1.5V

Since transconductance G_m is sensitive to the variation in device size, two boundaries of transition region (W ≈ L) and two extreme cases are defined by G_m measurements. As indicated by the results in Fig. 1, when the gate is wider than 1.4 μm, the transconductance in D-L MOSFETs can be approximated to that of normal MOSFET with L = L_D and W = $\sqrt{2}$ W_D. That is, the current path perpendicular to the gate electrode is dominant and channel widening effects efficient when $W_D \geq 1.4\mu m$. As the channel width is reduced, transconductance in D-L MOSFETs deviates from the relation; $G_m \propto W / L = (\sqrt{2} W_D) / L_D$. When the gate is narrower than 0.5 μm = ($1/\sqrt{2}$) L_D, the transconductance in D-L MOSFETs with W = W_D and L = 1.0 μm = $\sqrt{2}$ L_D. In other words, current flows along the active area and channel lengthening effect is efficient if $W_D \leq (1/\sqrt{2}) L_D$. The boundary is $W_D = (1/\sqrt{2}) L_D$ for D-L MOSFETs and more generally $W_D = L_D \cos\theta$ for MOSFETs whose active area is inclined to the gate at angle θ.

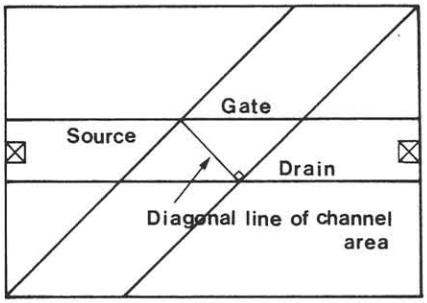

Fig. 3 The layout of diagonal-layout MOSFETs at the transition point.

This boundary condition makes the configuration in which the perpendicular from drain to source coincides with the diagonal line of channel area (see Fig. 3). The transition region is ($1/\sqrt{2}$) $L_D \leq W_D \leq 2L_D$. For this case, current flows as shown in Fig. 2 (b).

Three Dimensional effects

In normal MOSFETs, transconductance is proportional to W / L even in the deep submicron region. On the other hand, threshold voltage and ionization rate show drastic changes, as device size is reduced. These changes are caused by small size effects[3] such as short-channel effects and narrow-channel effects.

In D-L MOSFETs, the device size dependence of threshold voltage and ionization rate can not be explained by small size effects only. The concentration profile of boron diffused from the field region and electric field distribution in the substrate should be taken into consideration. That is, "*three dimensional current path modulation*" should be considered.

The threshold voltage V_{th} in D-L MOSFETs with 0.5-μm-wide channel width is measured under the bias condition V_{DS} = 3 V and V_{BB} = -3V. The threshold voltage V_{th} is defined as the gate voltage that gives 10-nA drain current. For comparison, the channel length L_D dependence of threshold voltage of normal MOSFETs was also measured.

As can be seen in Fig. 4, the threshold voltage shift due to short-channel effects in D-L MOSFETs is small, even with submicron channel length at which the V_{th} of normal MOSFETs becomes fairly low. The

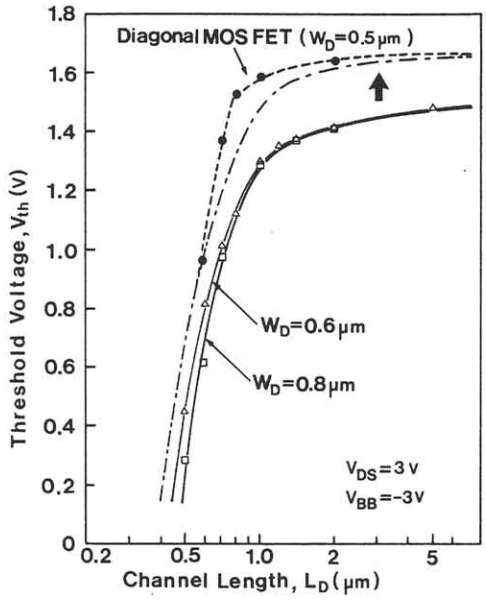

Fig. 4 Threshold voltages as a function of channel length. The chain line indicates the normal MOSFET line (W_D = 0.6 μm) displaced upward for comparison with the diagonal-layout MOSFET line.

channel lengthening effect reduces the electric field strength at the drain and suppress the short-channel effects; this provides the flat V_{th}-L_D property. However, in the short channel region (L_D < 0.8 μm), the channel lengthening effect gradually decreases and V_{th} approaches the value of the normal MOSFETs.

As for the V_{th}-W_D property, threshold voltage in both normal MOSFETs and D-L MOSFETs increase in a narrow channel region below 2 μm. (see Fig. 5)

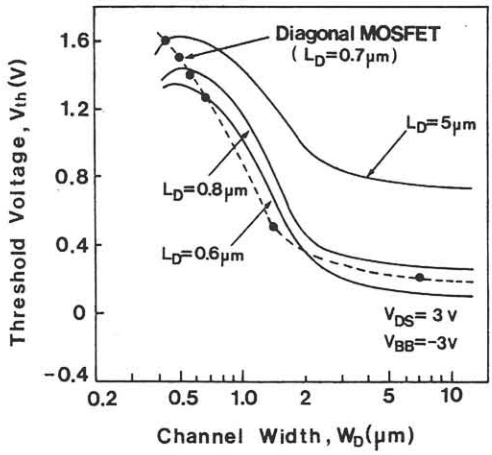

Fig. 5 Threshold voltages in the diagonal-layout MOSFETs and normal MOSFETs as a function of channel width.

The threshold voltage increases are mainly caused by field boron diffusion, because the bird's beak intrusion length is estimated from the G_m measurements to be 0.1 μm in normal MOSFETs.

In ultra narrow-channel region ($W_D \leq 0.5$ μm), the threshold voltage in normal MOSFETs saturates and then decreases because of inverse narrow-channel effects[4], whereas the threshold voltage in D-L MOSFETs continues to increase. This is because the channel lengthening effects overcomes inverse narrow-channel effects.

Figure 6 shoes the channel width dependence on ionization rate, i.e., (the peak substrate current I_{BB}^{max}) / (the source current I_S). The MOSFETs were subjected to bias conditions of $V_{DS} = 5$ V and $V_{BB} = -3$ V.

In normal MOSFETs, the ionization rate increases in the narrow channel region is also caused by field boron diffusion which makes the electric field at the drain high. When the channel width becomes wider than 0.5 μm, the D-L MOSFETs behave like normal MOSFETs. However, ionization rate in D-L MOSFETs suddenly decrease at $W_D = 0.5$ μm. This result indicates that the channel lengthening effect reduce the electrical field at the drain and suppresses hot carrier generation. The boundary channel width ($W_D = 0.5$ μm $= L_D/\sqrt{2}$) is consistent with the result derived from the G_m measurement.

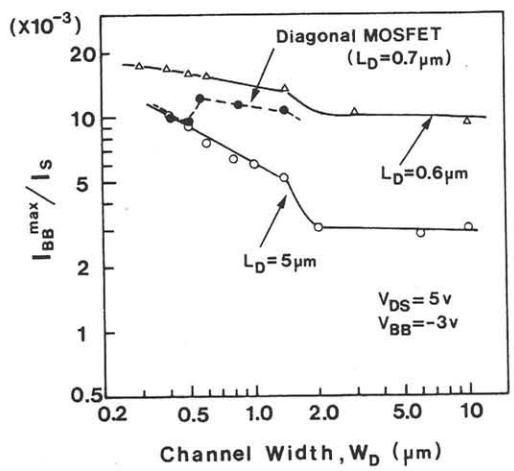

Fig. 6 Channel width dependence on ionization rates in diagonal-layout MOSFETs and normal MOSFETs.

Conclusions

The effects of being set an active area diagonally across a gate electrode in submicron MOSFETs were investigated. It is shown that submicron diagonal-layout MOSFETs have desirable characteristics as follows. The threshold voltage shift in short channel region is reduced, very small hot carrier generation is realized, and inverse narrow-channel effects are suppressed.

According to transconductance measurements and three-dimensional numerical analysis, it is found that current path in diagonal-layout MOSFETs depends on the ratio of channel width and channel length. This current path modulation causes the three dimensional effects which gives the good characteristics described above in the range $L_D \geq \sqrt{2}\, W_D$.

Acknowledgment

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