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Multilayered Well Formation for Sub-0.5 μm CMOS Devices Utilizing High Energy Ion Implantation

Kiyonori OHYU, Hidekazu GOTHO, Tadashi SUZUKI, and Nobuyoshi NATSUAKI
Central Research Laboratory, Hitachi, Ltd.
Kokubunji, Tokyo 185, Japan

A method for retrograde well and buried shield layer formation that utilizes high energy ion implantation is investigated for the multilayered wells of sub-0.5μm CMOS devices. Parastic bipolar actions can be effectively suppressed. The layers are shown to effect a decrease in the leakage current of pn junctions in the well. It is demonstrated that the present method has advantages over the traditional one based on thermal diffusion from both the standpoints of device properties and process control.

1. Introduction

High energy (MeV) ion implantation offers a flexible technique for doping impurities into the micron depth range of Si substrates. For this reason, MeV implantation has recently been investigated for use in various applications, especially, formation of retrograde wells and buried shield layers for latch-up protection and/or device isolation in CMOS LSIs[1,2]. To date, it has been reported that low dose implantation, which is used in well and shield applications, is free from detrimental residual damage and is potentially applicable to state-of-the-art VLSIs[3]. However, further investigation is still necessary to determine the feasibility of this technique for future sub-0.5μm CMOS devices. This is because a more sophisticated multilayered-well structure should be employed[4] and impurity profiles should be rigorously optimized to achieve device down-scaling.

This paper describes a multilayered well formation method that utilizes MeV implantation which is compared to the usual thermal in-diffusion one. It is shown that better device characteristics and process control are obtained with the MeV-implantation. The suppression of parastic bipolar actions and reduction in pn junction leakage current, induced by minority carrier diffusion in the bulk Si, are especially emphasized.

2. Experimental procedures

Performances for p- and n- type wells as well as n-type shield layers were evaluated in terms of pn junction, parastic bipolar transistor, and MOSFET characteristics. These characteristics were examined using the CMOS device shown in Fig. 1. The conventional CMOS device fabrication process is listed in Table 1. To retrograde the well, B and P implantations were performed after step (4) at 1 and 2 MeV, respectively, while the n-type shield layer was formed by P implantation at 4MeV. The above implantation doses were $1\times10^{13}/cm^2$. Subsequent annealing was done at 1000℃ for 10min in dry N_2. Implant and diffusion conditions in steps (2) and (3), were designed to meet 0.5μm CMOS device specifications.

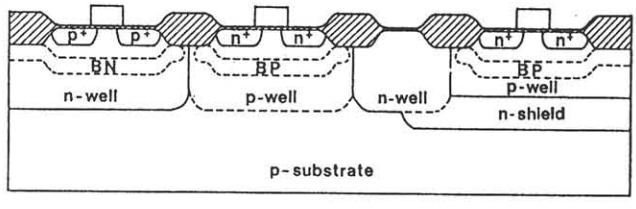

Fig. 1 Schematic of scaled-down CMOS device structure. MeV implantation is used for p- and n- retrograde wells and n-shield layer formation.

Table 1 Conventional process for CMOS device fabrication.

(1)	starting material ; 10Ω-cm, (100), p-type Si substrate
(2)	n-shield layer formation ; P implantation and driving-in diffusion
(3)	n- and p- well formation ; P and B implantations and driving-in
(4)	device isolation ; 550nm field oxidation by LOCOS method, p-buried (BP) layer formation by B implantation at range of 180~400keV, and n-buried (BN) layer formation by P implantation at range of 200~500keV
(5)	gate formation ; 16nm gate oxidation and n⁺-poly-Si (P-doped) deposition
(6)	junction formation ; As and B implantations, and activation annealing
(7)	passivation ; 400nm P-doped oxide (PSG) deposition
(8)	electrode formation ; 900nm aluminum (Al) deposition

3. Results and discussions

3.1 Retrograde well characteristics

The effects of well retrogradation on well resistance are shown in table 2. Retrograde well resistance was less than 1/2 at a dose of $1\times10^{13}/cm^2$ when compared to that for a controlled (diffused) well. As a consequence, when the p-type well acted as the base region for a parastic bipolar transistor, the static common-emitter current gain (β) was decreased to about 1/3 by retrograde well formation. In addition, no degradation of well surface properties was seen during MeV implantation was not seen.

Fig. 2 shows the reverse bias voltage dependence of pn junction leakage currents at room temperature. In the figure, leakage currents are separated into two components in a normalized from: an area component (leakage current through the junction bottom) and a perimeter component (leakage current through the junction side wall). It can be seen that the perimeter component is not influenced by well retrogradation. In contrast, the area component decreases to about half in retrograde wells. This area component reduction is seen over the whole measurement temperature range of 25~150℃, as shown in Fig. 3. From these results, it can be concluded that the generation current in the depletion layer and the diffusion current from the neutral region are decreased by retrograde well formation.

Table 2 Retrogradation effect for well resistance.

	well resistance	
	n-well	p-well
control (diffusion)	1.2kΩ/□	3.0kΩ/□
retrograde ($1\times10^{13}/cm^3$)	0.5kΩ/□	1.4kΩ/□

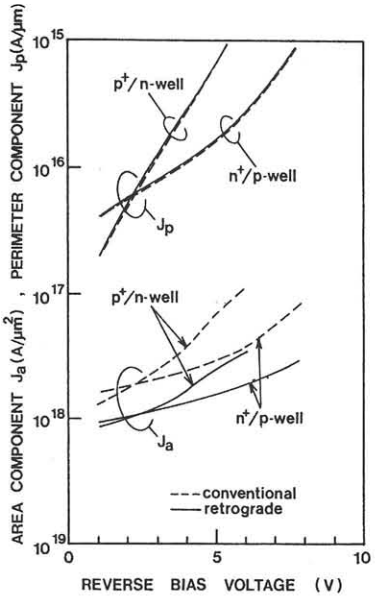

Fig. 2 Reverse bias voltage dependence of pn junction leakage current at room temperature.

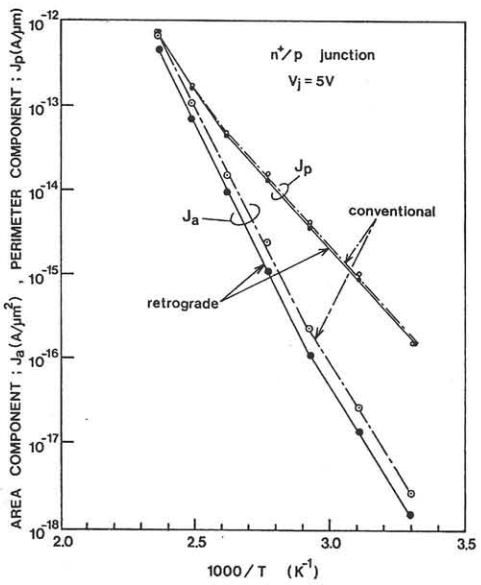

Fig. 3 Temperature dependence of area and perimeter components of leakage current at 5V.

The reason for this occurs may be as follows. First, extension of the depletion layer width is suppressed by the increase in well dopant concentration when the retrograde well is formed. Second, diffusion of the minority carrier in the well is suppressed by a potential barrier that is formed by the MeV implanted layer.

Fig. 4 shows drain breakdown voltage for nMOSFETs as a function of channel length. It can be seen that BV_{DSO}, depending on the punch-through or avalanche breakdown phenomena, is not influenced by retrograde well formation. In contrast, $BV_{DS(min)}$, depending on the parastic bipolar action, increases in a retrograde well. It is understood from this result that only parastic bipolar action in MOSFETs is suppressed by a reduction of in well resistance due to retrograde well formation.

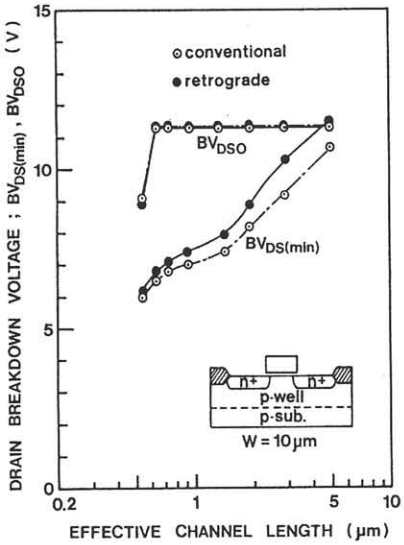

Fig. 4 Drain breakdown voltage as a function of channel length for nMOSFETs.

3.2 n-type shield layer characteristics

When the shield layer was formed by MeV implantation, resistances of the p-type well and the n-type shield layer were lowered, as shown in Table 3. P-well resistance is strongly dependent on the n-shield layer formation method. Table 3 results that p-well hole concentration in the control sample apparently decreased due to carrier compensation by P diffusion, while the concentration decrease for the MeV implanted sample was quite small. Thus, MeV implantation for n-shield layer formation has little effect on p-well resistance. Moreover, resistance of the n-shield layer formed by MeV implantation can be easily decreased in comparison with the control sample. Actually, under practical device operating conditions, where the shield layer was biased to 5V, resistance remained low by a factor of 1/4. Consequently, β for a parastic bipolar transistor whose base was the shield layer decreased to 1/3, as shown in Table 3. From the above results, it is expected that MeV implantation can effectively suppress parastic bipolar action in the multilayered well useful for sub-0.5μm CMOS devices.

Fig. 5 shows threshold voltage vs. channel length relationship for nMOSFETs formed in p-wells; without any shield layer, where the shield layer was formed by MeV implantation, and where the shield layer was formed by diffusion. In the case of the diffussed shield layer, threshold voltage decreased by about 0.05V when compared with that for the control sample having no n-shield layer. However, in the case of the MeV implanted n-shield layer, the reduction was almost the same as that for the control sample. Namely, the surface carrier concentration of the p-well is hardly affected by shield layer formation utilizing MeV implantation.

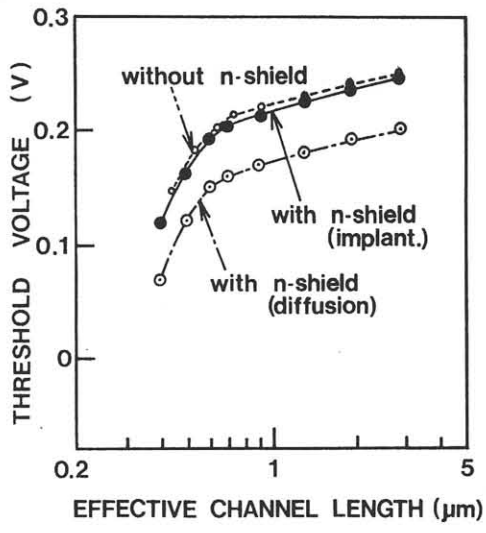

Fig. 5 Threshold voltage as a function of channel length for nMOSFET.

Table 3 Changes in well and shields layer resistance, and β of parastic bipolar transistor by n- shield layer formation conditions.

	p-well resistance	n-shield resistance 0V	n-shield resistance 5V	β
control (diffusion)	1.34kΩ/□	0.6kΩ/□	1.3kΩ/□	62
implant (1×10^{13}/cm^3)	1.26kΩ/□	0.2kΩ/□	0.3kΩ/□	20

Fig. 6 shows leakage currents of 160x160μm^2 n^+/p junction diodes as a function of measurement temperatures. A bias condition is also shown in the figure. In the sample having its n-shield layer formed by diffusion, leakage current is governed by minority carrier diffusion because activation energy, as estimated by the line slope, is about 1.2eV. In the sample with its n-shield layer formed by MeV implantation, leakage current at higher temperatures due to minority carrier diffusion decreased to about 1/3 when compared with the diffused shield layer case. These results are explained as follows. Diffusion current is decreased by increasing the majority carrier concentration in the well and/or making a sink for minority carriers under the well if the minority carrier diffusion length is larger than the well width. When MeV implantation is used for shield layer formation, carrier compensation in the well is minimized and sufficiently heavy doping of the shield layer is achieved. This provides the necessary conditions for leakage current reduction.

From these results, it can be concluded that n-shield layers formed by MeV implantation can be successfully employed to improve device characteristics and at the same time assure a high degree of control in multilayered well tailoring.

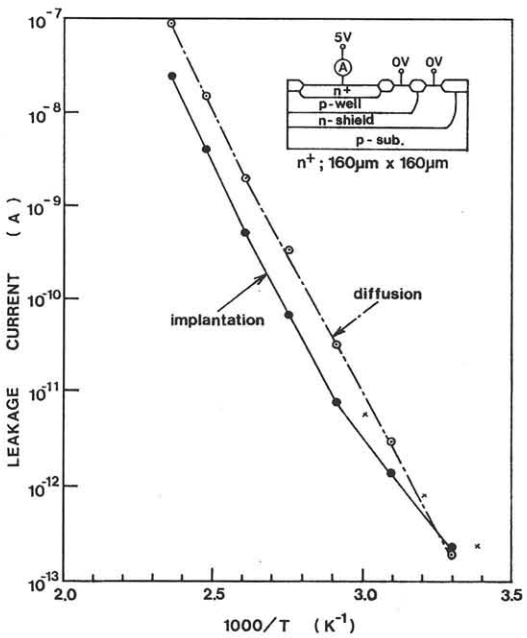

Fig. 6 Leakage current of n^+/p junction as a function of temperature.

4. Conclusion

The beneficial features of multilayered well formation that utilizes MeV implantation are summarized as follows. Lower resistances of MeV-ion implanted wells and shield layers lead to an improvement in latch-up immunity and drain breakdown voltage, both of which are governed by parastic bipolar action in scaled-down CMOS devices. Besides, the MeV implantation technique has the effect of decreasing the pn junction leakage current caused by minority carrier diffusion. In comparison with the conventional double in-diffusion technique, the MeV implantation technique has the advantages of precise and independent tailoring of the well and shield layer formation with a smaller thermal budget. Therefore, it can be concluded that the present method is a promising technique for developping scaled-down sub-0.5μm CMOS devices.

References

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