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CMOS Compatible Lateral Bipolar Transistor for BiCMOS Technology

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A CMOS-compatible lateral bipolar transistor having neither an epitaxial layer nor n^+ buried layers is proposed as a result the following investigation. A BiCMOS gate delay is not influenced greatly by the base width, W_B (i.e. by f_T, since $f_T \propto 1/W_B^2$) because of a large injection of minority carriers. Therefore low f_T (low cost) bipolar transistors can be useful for BiCMOS gate circuits. The obtained values of h_{fe}, f_{Tmax} and r_{bb} are 40, 2.3 GHz and 99 Ω, respectively.

1. Introduction

Recently, the drive to increase the speed performance of computers has accelerated the importance of high-speed, large-scale memories. BiCMOS technologies are very promising for this application since they offer the high drive capabilities of bipolar transistors while retaining the inherent low power consumption and high level of packaging density provided by CMOS.[1][2] Most existing BiCMOS processes, however, make use of a high performance vertical bipolar transistor which results in a rather complex and high cost process due to the incompatibility of the two types of transistors. The high performance vertical bipolar transistors used for BiCMOS LSIs require n^+ buried layers and an epitaxial silicon layer.

Usually, the speed performance of bipolar transistors is estimated by the f_T-I_c characteristic. Therefore high f_T transistors are regarded as necessary for high speed BiCMOS LSIs. The authors have noticed, however, that f_T does not have a great effect on BiCMOS gate delay time.

This paper describes the investigation by computer simulation of factors which influence the delay time in BiCMOS gate circuits. In accordance with the above investigation, a new lateral bipolar transistor for a BiCMOS gate having neither n^+ buried layers nor an epitaxial silicon layer is proposed and is actually fabricated. Some properties of the bipolar transistor are also reported.

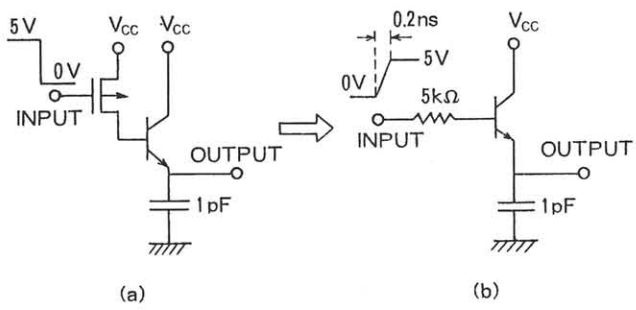

Fig. 1. (a) BiCMOS gate circuit, and (b) its equivalent circuit for computer simulation.

2. Proposal of a new lateral bipolar transistor for BiCMOS gates

2.1 Essential factors of BiCMOS gate delay

It has been determined by experiment that BiCMOS gate delay, t_{pd} can be improved when the thickness of the epitaxial silicon layer, d_{epi} is decreased. First, the dependence of bipolar transistor properties and t_{pd} on d_{epi} are investigated by computer simulation (transient analysis).

The equivalent circuit of a BiCMOS gate for simulation is shown in Fig. 1. The MOS transistor of the BiCMOS gate is replaced with a 5 kΩ resistor in the equivalent circuit. It is assumed that the input voltage has a 0.2 ns delay.

Figure 2 shows the simulated f_T-I_C characteristics and the simulated dependence of I_E, and I_B on time for various d_{epi}. Moreover, the simulated dependence of maximum cutoff frequency, f_{Tmax}, maximum emitter current, I_{Emax} and t_{pd} on d_{epi} is shown in Fig. 3. Here t_{pd} is defined as the time during which output voltage rises from 0 V to 4.5 V. The thinner d_{epi} is, the shorter the distance between emitter and collector, d_{E-C}, and consequently the depletion layer of the collector region also becomes thin. Thus f_T becomes large when d_{epi} is decreased. The electric field intensity between emitter and collector also increases. Therefore I_E increases when d_{epi} is decreased, and consequently t_{pd} is improved.

Next, the relation between t_{pd} and base width, W_B is investigated. Figure 4 shows the simulated dependence of t_{pd} and f_{Tmax} on W_B. It is well known that high speed bipolar transistors usually have high f_{Tmax}. Conversely, as W_B becomes small, f_{Tmax} increases abruptly, while t_{pd} increases slightly in the BiCMOS gate circuit. The reason for this is described as follows.

In BiCMOS gate circuits, the base-voltage changes from 0 to +5 V or +5 to 0 V, depending on the input voltage. Therefore a high-level injection of minority carriers occurs from emitter to base. In such a case, the depletion layer of the collector region is distinguished by the injection of a large number of minority carriers. As a result, effective base width, $W_{B(eff)}$ determined by carrier concen-tration is widened by the increase of carrier concentration at the base-collector junction, as shown in Fig. 5(a). Thus t_{pd} does not depend very much on W_B, determined by impurity concentration, while it does depend on $W_{B(eff)}$ in high-level injection.

On the other hand, f_T is measured with a small signal circuit and therefore a high-level injection does not occur, as shown in Fig. 5(b). Consequently, f_T is approximately in proportion to $1/W_B^2$, and increases rapidly as W_B is decreased.

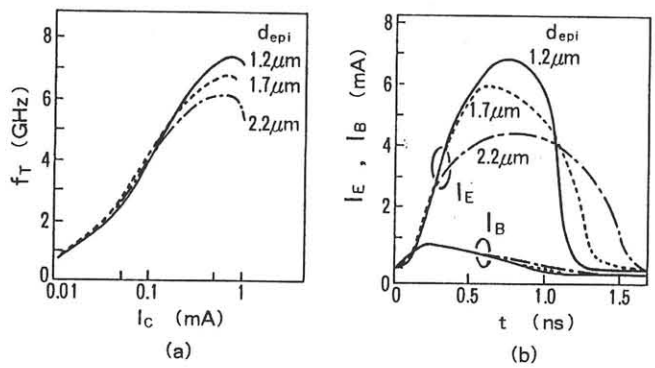

Fig. 2. Simulated f_T-I_C characteristics, and (b) simulated dependence of I_E, and I_B on time for various d_{epi}.

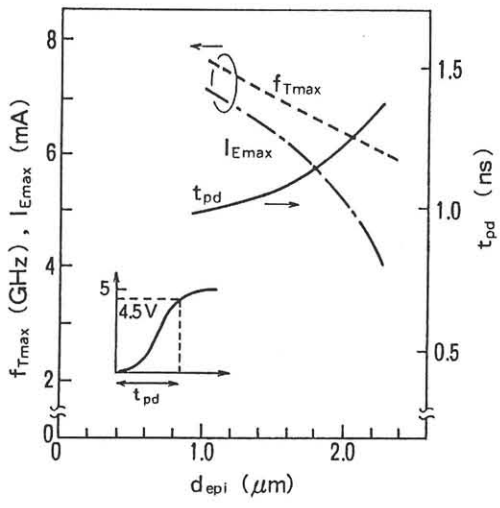

Fig. 3. Simulated dependence of f_{Tmax}, I_{Emax} and t_{pd} on d_{epi}.

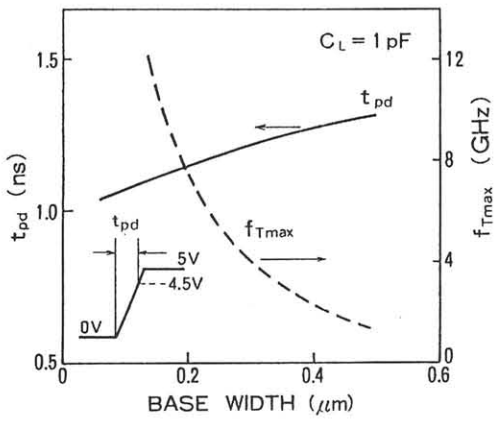

Fig. 4. Simulated dependence of t_{pd} and f_{Tmax} on base width, W_B.

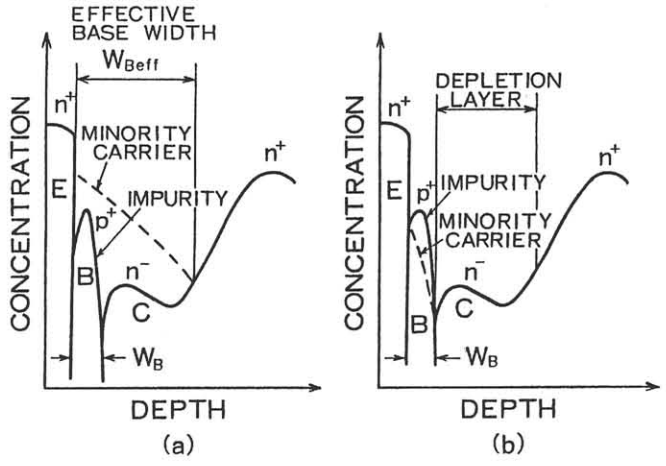

Fig. 5. Impurity and minority carrier profiles in case of (a) high-level injection, and (b) low-level injection.

2. 2 CMOS-compatible lateral bipolar transistor

It is found that the depletion layer of the collector region is distinguished by the high-level injection of minority carriers in the BiCMOS gate circuits, and consequently t_{pd} is dependent on $W_{B(eff)}$ (nearly equal to d_{B-C}). This suggests that it is possible to get high speed BiCMOS gate circuits even if lateral bipolar transistors are used, provided that the distance between emitter and collector is shortened by fine patterning technology. Therefore the authors propose that for BiCMOS gates, the CMOS-compatible lateral bipolar transistor be utilized, since it has neither an epitaxial layer nor n^+ buried layers. The structure of the transistor is shown in Fig. 6.

The self-alinged emitter/collector of the transistor are simultaneously formed by implantation similarly to self-alinged source/drain in MOSFET. Poly-silicon placed between emitter and collector is used as a base electrode. Low base resistance can be achieved by this structure. The width of p^+ base is nearly equal to that of a LDD spacer. The n^- collector of a vertical bipolar transistor is replaced by the p^- base. The p^- base and PWELL of NMOS are simultaneously formed by implantation.

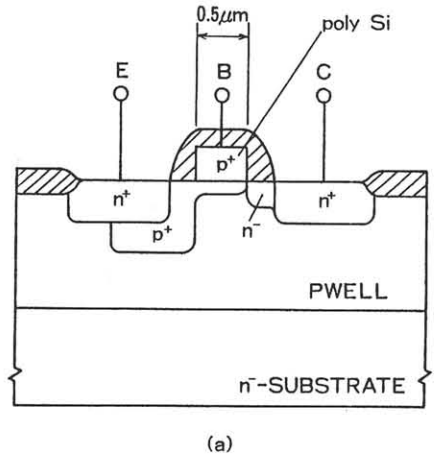

Fig. 6. Cross-sectional view of the CMOS-compatible lateral bipolar transistor.

2. 3 Bipolar transistor characteristics

Figure 7(a) shows the I-V characteristics of the lateral bipolar transistor. The Gummel plot of the same device is shown in Fig. 7(b), which indicates that h_{fe} is 188 (I_C =100μA), 40 (I_C =1 mA).

BV_{CEO}, BV_{CBO}, and BV_{EBO} are about 7, 6, and 6 V, respectively. BV_{CEO}, BV_{CBO} are almost same, since BV_{CEO} is determined by the base-collector junction breakdown voltage in the lateral bipolar transistor.

The f_T-I_C characteristics are shown in Fig. 8 which indicates that f_{Tmax} is 2.3 GHz at I_C = 3 mA. The obtained value of r_{bb} is 99 Ω.

3. Conclusion

It is found that delay time, t_{pd} does not depend very much on the base width W_B (and hence on f_T, since f_T $1/W_B^2$), determined by impurity concentration in BiCMOS gate circuits. This is because the depletion layer of the collector region is distinguished by the high-level injection of minority carriers. Consequently, t_{pd} is dependent on the effective base width, $W_{B(eff)}$ (nearly equal to the distance between emitter and collector, d_{E-C}).

This result suggests that it is possible to achieve high speed BiCMOS gate circuits even if lateral bipolar transistors are used, provided that d_{E-C} is shortened by fine patterning technology. Therefore the CMOS-compatible lateral bipolar transistor having neither an epitaxial layer nor n^+ buried layers is proposed and is actually fabricated.

The obtained values of h_{fe}, f_{Tmax} and r_{bb} are 40, 2.3 GHz, and 99 Ω, respectively.

The lateral bipolar transistor proposed in this paper should be useful for low-cost, high-speed BiCMOS gate circuits.

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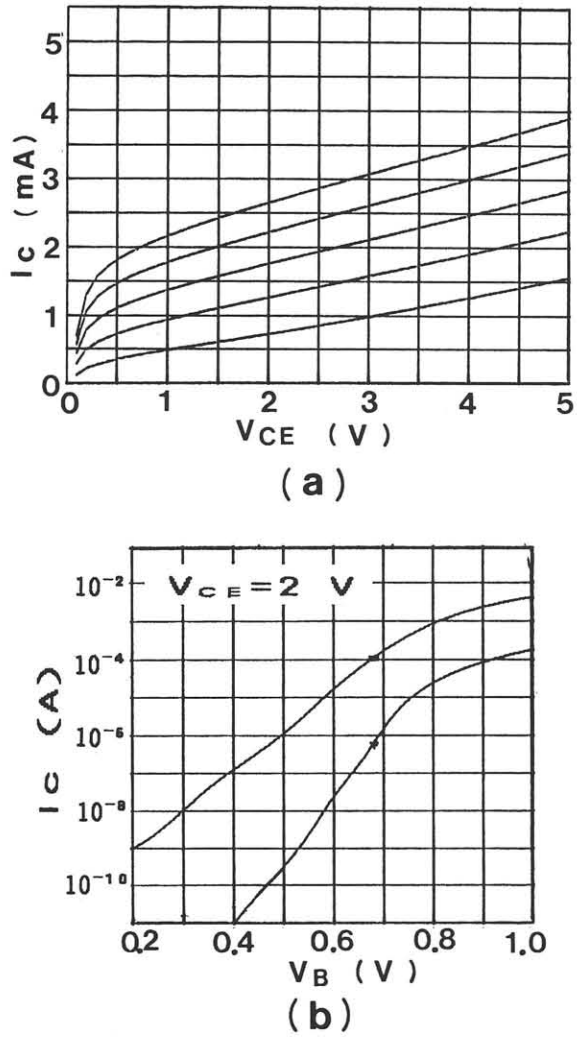

Fig. 7. (a) I-V characteristics, and (b) Gummel plot of the CMOS-compatible lateral bipolar transistor.

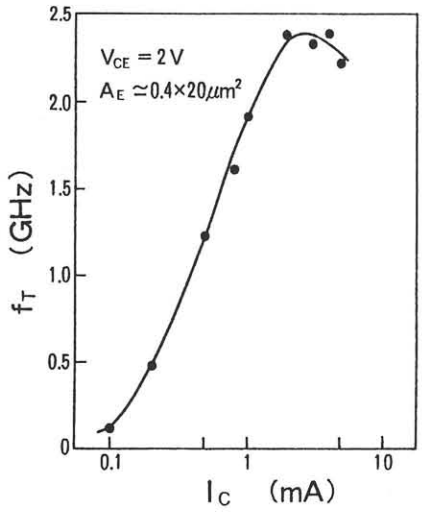

Fig. 8. f_T-I_C characteristics of the CMOS-compatible lateral bipolar transistor.