Limit on Triode Region Drivability for a 0.1 \( \mu \)m MOSFET, Predicted by Process/Device Simulation Including Parasitic Resistance

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A process/device simulation method which incorporate all the parasitic resistances has been developed. This has made it possible to analyze parasitic resistances with the same accuracy as for the channel resistance. Various shallow source/drain fabrication processes were evaluated using this method.

The limitation in triode region drivability increase was analyzed quantitatively with the new method, considering all the limiting factors.

1. INTRODUCTION

MOSFET drivability increases with miniaturization. But there are two factors limiting triode region drivability increase. First is a relative increase in parasitic resistance. Fabricating a shallow source/drain diffusion layer is indispensable for further MOSFET miniaturization, while this creates substantial parasitic resistance. Second is mobility degradation.

Up to now, analyses of these factors limiting miniaturization have been based on an analytical model\(^1\). Quantitative analysis considering these limiting factors is required, since experimental fabrications of 0.1 \( \mu \)m channel length MOSFETs\(^2\) have already been started.

This paper reports a process/device simulation method which incorporates all these limiting factors. The triode region performance of MOSFETs with 0.1 \( \mu \)m channel lengths has been clarified by means of this, and the limits on drivability are discussed.

2. METHODS OF ANALYZING PARASITIC RESISTANCE

A precise analysis by simulation has been performed in order to analyze parasitic resistance as a function of position and to evaluate the process dependence of the parasitic resistance. This is because the conventional analysis using the current-voltage characteristic can only obtain the total parasitic resistance.

Since the diffusion current is dominant near the source/drain junction, resistance cannot be calculated from the potential based on the simple Ohm's law. However, the resistance as a function of position can be calculated based on the direct proportionality of resistance to the quasi-Fermi potential as follows.

Using \( \Phi_f \), the quasi-Fermi potential

\[
I_d = w \left[ \mu q n_x \nabla \Phi_f \right] dy
\]

\[
= w \left( d \Phi_f / dx \right) \int_{r}^{\infty} q n_x dy
\]

\[
\Phi_f / I_d = ( \int_{r}^{\infty} q n_x dy ) \frac{dx}{w}
\]

where, \( y \): depth, \( x \): along channel,
\( \mu \): mobility, \( q \): electric charge element,
\( n \): carrier density.

Figure 1 shows the result of resistance simulation. Parasitic resistance is broken down into several parts, corresponding to the Ng\(^1\) model and represented by the equivalent circuit shown in Fig. 1(c).

Previously, MOSFET source/drain contact resistance was dealt with by the Transmission Line Model\(^3\).

The new method distributes a specific contact resistivity \( \rho_c \) to each grid point on the electrode, as an exter-
nal resistance (Fig. 2(b)). This incorporates the analytical Transmission Line Model into the device simulation.

3. PROCESS/DEVICE SIMULATION OF PARASITIC RESISTANCE FOR SHALLOW SOURCE/DRAIN FABRICATION PROCESSES

The contribution of contact resistance becomes the largest within the parasitic resistance, because it is not reduced with the scaling down of a MOSFET. Therefore, it is indispensable to use a silicide contact. In the present method, using process/device simulation, the specific contact resistivity \( \rho_c \) is set between the diffused region and the silicide region, considering the 2-dimensional geometry of the silicide region.

Figure 3 compares simulated and measured contact resistance values for silicide contacts as a function of \( \rho_c \). Agreement between them is good.

Figure 4 shows the current flow in a 0.1 \( \mu m \) level MOSFET with a silicide contact.

The parasitic resistance values for some proposed shallow junction formation processes can be calculated as shown in Table 1. Experimental data are not necessarily obtained for optimal conditions integrating the whole MOSFET fabrication process, so the process conditions for simulation and experimental data are not the same.

For an NMOS, the process proposed by Sai-Halasz\(^2\) for 0.1 \( \mu m \) MOSFET was scaled down including the contacts, and has been shown to have a very low parasitic resistance.

On the contrary, it is very difficult to fabricate a shallow (\( x_j=0.1 \mu m \)) source/drain junction for a PMOS and restrict parasitic resistance with present process technology.

Figure 5 compares the parasitic resistance to the intrinsic channel resistance in MOSFETs miniaturized to the 0.1 \( \mu m \) level. For an NMOS, the contribution of parasitic resistance remains below 30%, even if miniaturized to the 0.1 \( \mu m \) level. However, for a PMOS, the parasitic resistance easily surpasses 50%, unless a new process technique is developed.

4. LIMITING FACTORS ON TRIODE REGION DRIVABILITY

As for mobility degradation, we can summarize data using the effective normal electric field \( E_{\text{eff}} \),

\[
E_{\text{eff}} = q/\varepsilon_0 \varepsilon_{Si} \cdot (N_{d \text{Si}} + \eta N_s(V_g))
\]

where,

\[
\eta = \begin{cases} 
1/2 & (\text{NMOS}), \\
1/3 & (\text{PMOS}) 
\end{cases}
\]

As shown in Fig. 6, measured mobility\(^6\) can be plotted on a universal curve. The substrate impurity concentration for a 0.1 \( \mu m \) MOSFET increases to nearly \( 10^{13} \text{ cm}^{-3} \). In such a case, the contribution to \( E_{\text{eff}} \) from just the depletion charge itself reaches \( 5 \times 10^5 \text{ V/cm} \). Therefore, for an NMOS, rapid mobility degradation already begins in the weak inversion region. And for a PMOS, mobility degraded to nearly 80 \text{ cm}^2/\text{V·sec}.

The upper limits for triode region drivability can be predicted by combining the results mentioned so far. The inverse of conductance as a function of channel length showed linearity. This linearity changed, as shown in Fig. 7 with design rule reduction. The slope (inversely proportional to mobility) increased due to mobility degradation, although intercept (parasitic resistance) decreased when miniaturized to 0.1 \( \mu m \). Therefore, a minimum for the inverse of conductance existed. This means an upper limit for triode region drivability.

This limitation will come earlier for PMOS, unless a process technique to lower parasitic resistance can be realized.

5. DISCUSSION AND CONCLUSION

A process/device simulation method was developed to evaluate all the parasitic resistances. This has made it possible to analyze parasitic resistances with the same accuracy as for the channel resistance.

Various shallow source/drain fabrication processes were evaluated using this method.

The limitation on triode region drivability increase was analyzed quantitatively with the new method, considering all the limiting factors.

Furthermore, for 0.1 \( \mu m \) MOSFETs, a 100 A accuracy for the channel length is required. In Fig.7, the offset value \( \Delta L \) for the channel length represents the length of the accumulation resistance region at the edge of the source/drain. As shown in Fig. 7, this length \( \Delta L \) surpassed 100 A. In other words, this region is occupied by one impurity ion. This is because for 0.1 \( \mu m \) MOS-
FETs the impurity concentration of the substrate and source/drain edge is as high as $10^{16}$ cm$^{-3}$, and the mean distance between each impurity ion is 100 Å.

To determine the channel length and to evaluate the parasitic resistance are two sides for defining a MOSFET. Up to now, it is not sufficient to clarify the relation between them and determine each value definitely. Especially, when comparing experimented and simulated MOSFET characteristics, the correspondence between the experimental effective channel length and the geometrical channel length used in simulation has not been cautiously considered.

However, as mentioned so far, it is necessary with miniaturization to the 0.1 μm level to treat a MOSFET with a resolution of 100 Å or one impurity ion.

Moreover, in such a case, the fluctuation of impurity distribution affects the characteristics of a MOSFET.

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![Fig.1 Results of parasitic resistance extraction. (a)Analysis region, (b)resistance as a function of position, (c)equivalent circuit model representing parasitic resistance. Rco: contact resistance, Rsh: sheet resistance, Rsp: spreading resistance, Rac: accumulation resistance, Rch: channel resistance.](image)

![Fig.2 Parasitic resistance treatment in present method. (a)Current flow in source/drain diffusion layer. (b)Specific contact resistivity $\rho_c$ is divided and attached to each grid point.](image)

![Fig.3 Contact resistance $R_{co}$ for silicide contact as a function of specific contact resistivity $\rho_c$. Experimental data are after Y.Taur.](image)
Table 1 Comparison of parasitic resistances for various shallow source/drain fabrication processes

<table>
<thead>
<tr>
<th>Process</th>
<th>Rco (Ω)</th>
<th>Rsh (Ω)</th>
<th>Rsp (Ω)</th>
<th>Total (Ω)</th>
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<tbody>
<tr>
<td>N MOS</td>
<td>17</td>
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<td>92</td>
<td>2400/Ω</td>
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<tr>
<td>P MOS</td>
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<td>13200/Ω</td>
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<table>
<thead>
<tr>
<th>RTA</th>
<th>13</th>
<th>95</th>
<th>60</th>
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Fig.4 Current flow in 0.1μm level MOSFET with silicide contact

Fig.5 Comparison between resistance components in 0.1μm level MOSFET, IVgl=1, tVd=0.1V, tVth=50 A, w=10 μm. Upper two were simulated by #1, #3 processes in Table 1, respectively.

Fig.6 Measured mobility as a function of effective normal field E_{eff}.

Fig.7 Trend of triode region drivability with design rule reduction. Inverse of channel conductance g_{ds} and mutual conductance g_{mn} as a function of channel length Lc.