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# High Drivability CMOSFETs with Asymmetrical Source-Drain (ASD) Structure for Low Supply Voltage ULSIs

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A new high drivability CMOSFET with asymmetrical source-drain (ASD) structure for future high-speed ULSIs is proposed. This structure is fabricated using an additional ion implantation step for the source region after the LDD formation process. This structure has equal or better drivability as SD, the same reliability as LDD, sufficient process margin and no limitations, such as short channel effect and gate-induced junction current. Therefore, an ASD structure with a minimum design gate length can be used, and the parasitic capacitance doesnot increase. A higher circuit operation speed can be obtained, if this ASD structure is used in low supply voltage ULSIs.

## 1. INTRODUCTION

In the future half or subhalf micron CMOSFETs used in ULSIs will operate under low supply voltage. The reason for this is device reliability can be maintained. However, current drivability of CMOSFETs decreases. Therefore, in high-speed ULSIs, such as high-speed SRAMs, a higher drivability is required.

Recently, two typical structures that have high drivability were reported. The first is a gate source-drain overlapped LDD structure [1-4], which has not only high drivability but also high reliability. This device can be used for high supply voltage ULSIs. However, if this device is used in low supply voltage ULSIs, high speed operation cannot be achieved because the parasitic capacitance (gate source-drain overlap capacitance) increases. The second is a lightly-doped drain (LDD) structure with a source that changes from a lightly-doped source region to a heavy-doped region[5]. This device has high drivability and the same reliability as a conventional LDD MOSFET. Therefore, by using this device in low supply voltage ULSIs, high speed operation can be achieved. However, if this device is scaled down, serious limitations emerge such as short channel effects and gate-induced junction leakage current. Therefore, the source structure of this device needs to be modified and optimized.

In this paper, we propose a new high drivability CMOSFET with an asymmetrical source-drain (ASD) structure and discuss its characteristics. This ASD structure is fabricated using an additional ion implantation step ( ASD implantation ) before/after the spacer formation ( called ASD I and ASD II respectively ) into the conventional LDD fabrication process. The comparison between ASD I and II is also discussed. Moreover, circuit performance is described when these devices are applied to a ring oscillator.

## 2. DEVICE STRUCTURE AND FABRICATION PROCESS

Schematic source cross sections of ASD structures are shown in Fig.1. The ASD structure is fabricated by an additional ion implantation step of photoresist mask for the source side of a LDD MOSFET. The drain of the ASD structure is a conventional LDD structure, but the source is a single-drain (SD) structure. In particular, the heavy-doped source that previously existed, becomes a more heavy-doped source region. ( $n^{++}$, $p^{++}$ in Fig.1 ) The ASD structure is fabricated using two processes; ASD I and II. ASD I is fabricated using an additional ASD implantation step, which is carried out before the LDD spacer formation. The dopant ions of n-channel and p-channel for ASD I are $As^+$ and $B^+$, respectively. On the other hand, ASD II is fabricated using an additional ASD implantation step, which is carried out after the LDD spacer formation. The dopant

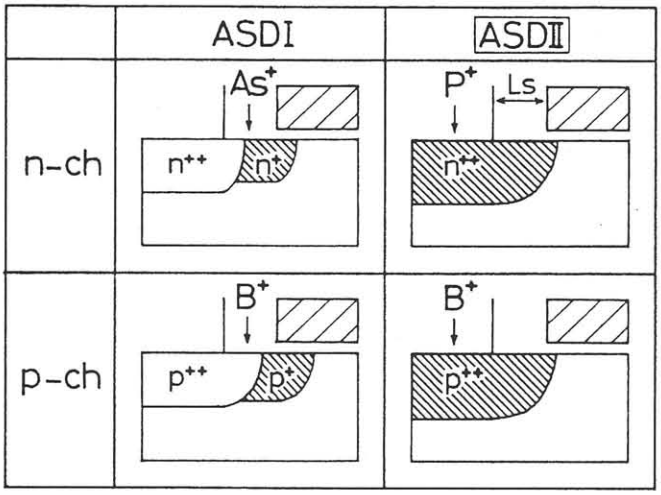


Fig.1 Schematic Source Cross Sections of ASD I, II Structure. Each arrow shows the Location of Additional ASD Implantation and the Dopant Ions.

ions of n-channel and p-channel for ASD II are $P^+$ and $B^+$, respectively. The ASD implantation dose is $0.1\sim5\times10^{15}cm^{-2}$. The ASD II structure can use a dopant ion with a larger diffusion coefficient. The gate oxide thickness is 15 nm. The gate electrode is policide ( WSi/poly-Si ). The LDD spacer length Ls, which is the key parameter in ASD II, is 0.19 ~ 0.23 $\mu$m. The dose for the lightly-doped drain region is $1\times10^{13}cm^{-2}$( $n^-$ or $p^-$ in Fig.1 ).

The low supply voltage $V_{DD}$ used in measuring the device characteristics is 4V. This voltage is the maximum allowable supply voltage determined by the hot-carrier breakdown-voltage in an n-channel LDD MOSFET with a 0.5 $\mu$m gate length.

## 3. RESULTS AND DISCUSSIONS

### A. Comparison between ASD I and II

The short channel effect is one of the more serious limitations in ASD devices. The threshold voltage lowering ( $V_{TH}$ vs. $L_G$ ) characteristics of n-channel and p-channel of an ASD structure are shown in Fig.2. It is found that threshold voltage lowering is more severe in both ASD I and II, as the ASD dose increases. In the p-channel, threshold voltage lowering in ASD I is more severe than in ASD II. This is because the source juncton depth increases, and the effective channel length decreases. Therefore, this indicates an upper limit for the ASD dose.

Gate-induced junction leakage current is also a serious limitation. This current flows because of band-to-band tunneling at the junction edge under the gate electrode[6,7]. Source junction leakage currents of n-channel of an ASD structure and LDD are shown in Fig.3. It is found that as the ASD dose increases, the rise-voltage, in which this leakage current rises sharply, is lower in both ASD I and ASD II. It is obvious that the rise-voltage of ASD II is higher than ASD I. As the ASD dose increases, this leakage current increases because the junction electric field increases.

Consequently, ASD II can avoid the above-mentioned limitations, but doses have an upper limit. The maximum allowable ASD dose of n-channel and p-channel for ASD II with Ls= 0.2 $\mu$m is $2\times10^{15}$, $4\times10^{15}cm^{-2}$, respectively. It should be noted that these ASD doses depend on the spacer length. ASD II can use a dopant ion with a larger diffusion coefficient, such as $B^+$ and $P^+$. As a result, ASD II reduces the junction electric field and maintains the short channel effect. ASD II has a greater process margin since it has a good resistration tolerance of photolithography to the spacer length.

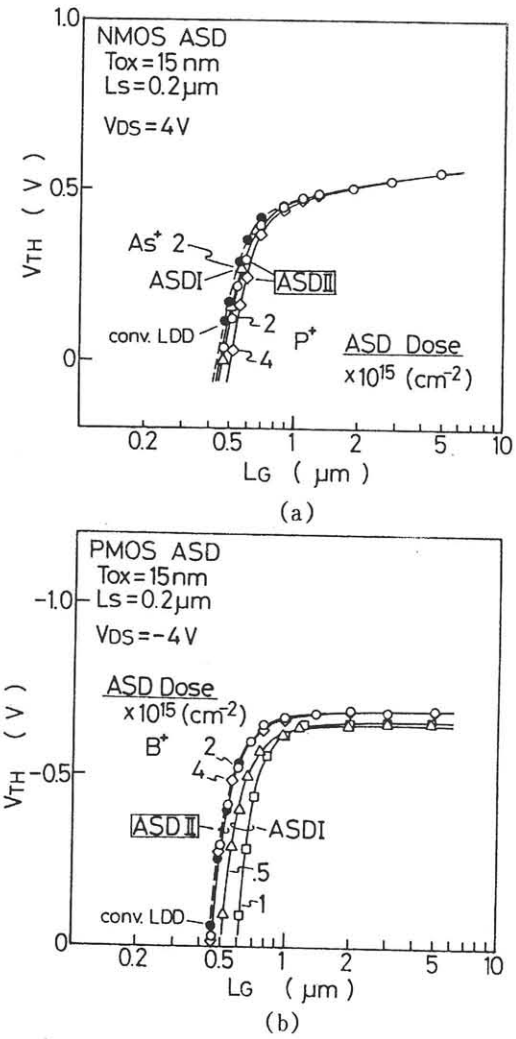


Fig.2 Threshold Voltage Lowering for (a) n-channel, (b) p-channel ASD I, II vs. Gate Length.

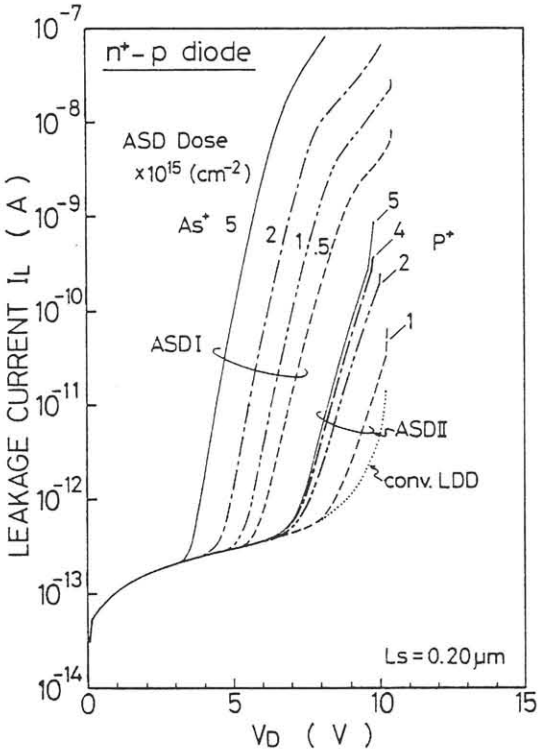


Fig. 3 Gate-induced Junction Leakage Current for n-channel ASD I, II. The Structure is $n^+$-p Diode with Gate Biased 0V.

B. Current Drivability of ASD II

Increase-rates of drain saturation current, $\Delta I_D/I_{D_0}$ vs. ASD dose in a Leff = 0.5 $\mu$m ASD structure with several spacer-lengths are shown in Fig. 4. The solid lines are for n-channel, and the broken lines are for p-channel. As the ASD dose increases, this rate increases in p-channel, but saturates in n-channel.

The source-drain series resistance Rex of ASD II vs. ASD dose is shown in Fig. 5. This resistance is estimated by channel-resistance measuremant at a low gate bias voltage [8]. Rex decreases as the ASD dose increases. However, the reduction of Rex in n-channel saturates to a level where the resistance of the lightly-doped source region can be neglected. On the other hand, Rex in p-channel decreases below this level, and doesnot saturate. This is because not only the $p^-$ layer resistance decreases, but also the resistance of heavy-doped source region $p^+$, which previously existed decreases. If the resistance of the lightly-doped source region disappears, the drain saturation current reaches a current level of a SD structure. Consequently, the drain saturation current of n-channel and p-channel ASD II increases to the level of a SD structure and to more this level, respectively. These increase-rates are about 5~10% in the maximum allowable ASD dose.

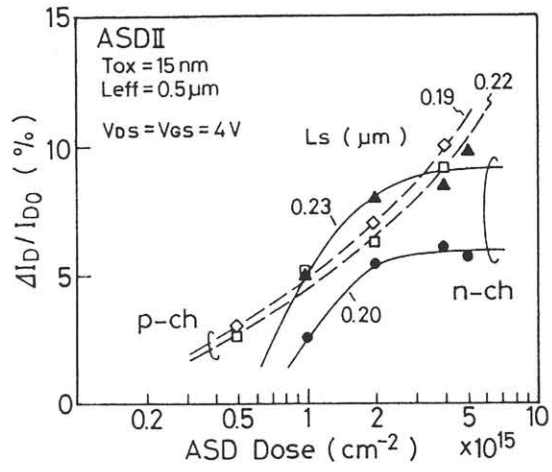


Fig. 4 Drain Satulation Current Increase-rate for ASD II vs. ASD Dose.

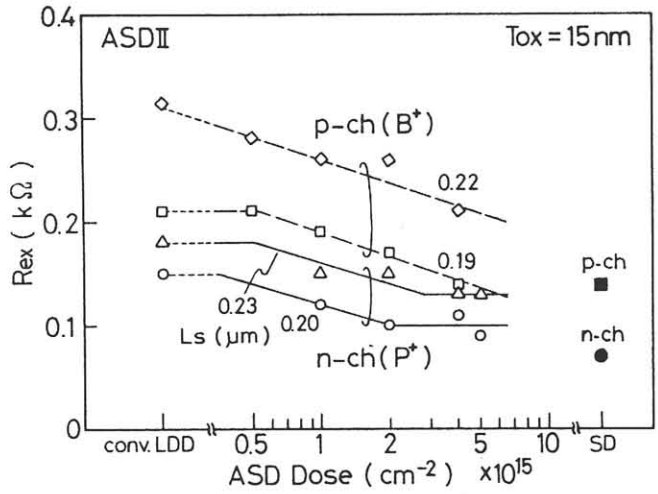


Fig. 5 Source-drain Series Resistance vs. ASD Dose for ASD II, LDD and SD Structure.

C. Hot-Carrier Reliability

The substrate current, which can be a monitor of the hot-carrier generation current, increases in ASD II, because the channel current increases. Consequently, Gm degradation for ASD II increases more than LDD. However, both structures have a different criterion for evaluating hot-carrier effects. In general, Gm degradation in the LDD is measured in the reverse-mode connection (source-drain connection is reversed after stressing). In ASD II, however, it is measured in the normal-mode connection (source-drain not reversed). This is because ASD is not used with the reverse-mode connection.

The Gm degradation rate, $\Delta Gm/Gm_0$, which is measured using these criterions, vs. stress time in typical n-channel ASD II and

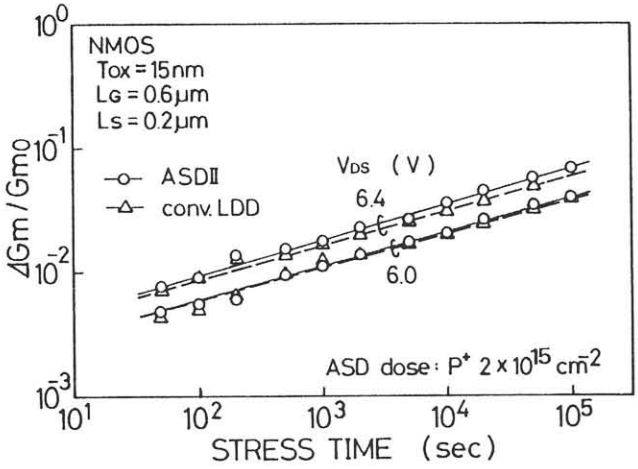


Fig.6 Gm Degradation Rate vs. Stress Time for Typical ASD II and LDD.

LDD is shown in Fig.6. The Gm degradation difference in this strucure is small. It is found that ASD II has the same reliability as conventional LDD. This reliability is sufficient for a 4V operation.

D. Circuits Application and Performance

ASD devices are mainly applied on logical circuits, because the source-drain connection of ASD doesnot change. ASD and LDD are used in a 401-stage CMOS ring oscillator with fun-in/out=1 condition. The delay time per gate of these ring oscillators vs. the supply voltage is shown in Fig.7. The decrease-rate of the delay time is about 10%, which is equivalent to the drain current increase-rate.

Moreover, by using these devices in memory ULSIs, not only the operation speed of the peripheral circuits is faster, but also the memory cell performance is improved. In particular, ASD is very useful in high-speed SRAMs. This is because the resistance of the ground line in the memory cell is lower, and the drain-current ratio between a driver-gate MOSFET and a transfer-gate MOSFET is larger in SRAM memory cells. In particular, the latter can lead to a reduction in the memory cell area.

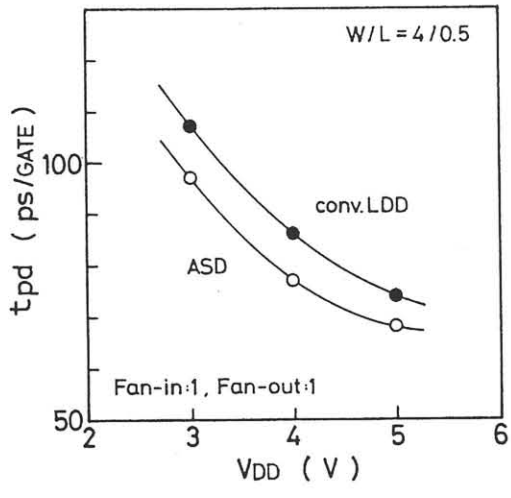


Fig.7 Delay Time Per Gate for 401-stage CMOS Ring Oscillator vs. Supply Voltage.

4. CONCLUSION

A new high drivability CMOSFET with an ASD structure has equal or better drivability as SD, sufficient process margin and no limitations in the submicron region. Therefore, an ASD structure with a minimum design gate length can be used, and parasitic capacitance doesnot increase. If ASD is used in low supply voltage ULSIs, a higher circuit-operation speed is obtained. In particular, ASD is effective for future memory ULSIs using high-speed operation.

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