Effect of InGaAs Well Width on Low-Noise Performance in AlGaAs/InGaAs Pseudomorphic HEMT

Masaaki Itoh, Kazuhiko Ohmuro, Hiroshi Nakamura, Seiji Nishi and Seiichi Takahashi

Research Laboratory, Oki Electric Industry Co., Ltd 550-5 Higashiasakawa, Hachioji, Tokyo 193, Japan

Abstract

We report the microwave performance of AlGaAs/InGaAs pseudomorphic HEMT with a $0.2\mu m$ gate. A new gate fabrication process was developed, which include two layer resists, an angle evaporation and reactive ion etching. By using this technique, we examined the effect of InGaAs well width on low-noise performance and InGaAs well width was optimized to minimize a noise figure. As a result, the fabricated HEMT with InGaAs thickness of 90Å exhibited an f_{Tmax} of 88.4GHz and an excellent noise figure of 0.49dB at 12GHz.

1.Introduction

Recently AlGaAs/InGaAs pseudomorphic high electron mobility transistors(HEMTs) have been demonstrated to have superb low-noise and power performances in millimeter - wave frequency region ^{1), 2)}. Compared with conventional AlGaAs/ GaAs HEMTs, pseudomorphic HEMT has advantages of the higher carrier density of the twodimensional electron gas(2DEG), and the higher electron saturation velocity of InGaAs³⁾. In this lattice-mismatched system it is important to keep the thickness of strained InGaAs layer less than straindependent critical value⁴). The influence of the InGaAs well width on rf performance in pseudomorphic HEMT has been investigated⁵⁾, however, that on noise performance has not been studied yet.

In this paper we describe a new gate fabrication process which enables the formation of sub-quartermicron gate by conventional photolithography first. Then the effect of InGaAs well width on low-noise performance is discussed in AlGaAs/InGaAs pseudomorphic HEMT with 0.2µm gate.

2. Crystal Growth and Electrical Properties

The pseudomorphic HEMT structures were grown by molecular beam epitaxy on undoped LEC GaAs substrates. The growth temperature was 530° C. Al mole fraction in AlGaAs was 0.28 and In mole fraction in InGaAs was 0.20. To study the dependence of electrical properties of 2DEG on InGaAs well width, the epitaxial structure which consisted of undoped GaAs of 7000Å, undoped InGaAs, undoped AlGaAs of 60Å, n-AlGaAs (2x10¹⁸cm⁻³) of 700Å and undoped GaAs of 100Å was used.

The sheet carrier concentration (N_s) and Hall mobility (μ_e) were measured at room temperature and 77K using Hall measurement. Figure 1 shows the N_s and μ_e as a function of InGaAs well width. As shown in the figure, the N_s and μ_e show almost the same values in the region from 90Å to 180Å. In the region beyond 200Å, the μ_e abruptly degrades less than 10000cm²/Vs. This result shows that the critical thickness of the InGaAs layer is nearly 200Å, and it is in good agreement with the results reported by Anderson⁶.

In order to study the effect of InGaAs well width below the critical thickness, the InGaAs thickness of 0Å, 90Å and 180Å were used for the



Fig. 1 N_s and μ_e versus InGaAs thickness.

device fabrication. An undoped AlGaAs spacer layer was not used in device structure to attain high N_s. The measured N_s and μ_e were $1.2 \times 10^{12} \text{ cm}^{-2}$ and $20000 \text{ cm}^2/\text{Vs}$ for the structure without the InGaAs layer, and were $1.7 \times 10^{12} \text{ cm}^{-2}$ and $20000 \text{ cm}^2/\text{Vs}$ for the structures with the 90Å and 180Å InGaAs wells.

3. Device Fabrication

The schematic cross section of device structure is shown in Figure 2. The thick n⁺-GaAs top layer was used to reduce the source resistance. The gate metal was in contact with n-GaAs with low carrier concentration to reduce the gate leakage current. The first step in device fabrication was the isolation by oxygen ion implantation. Next, source and drain ohmic contacts were formed by alloyed Au/Ni/AuGe. Finally, the gate was formed. A new gate fabrication process was used, which is schematically shown in Figure 3. In this process SiN was deposited on the wafer and two layer photoresists were coated on it. An upper layer photoresist (LMR resist 7)) was developed to define gate pattern with 0.5µm width. Thin Al metal was evaporated at tilted angle of 20° (Figure 3(a)). As shown in the figure, the shadow of Al was formed on the lower resist, whose width was 0.2µm. The shadow region of the lower layer resist was then removed anisotropically by reactive ion etching using O₂, and subsequently SiN was etched off







Fig. 3 Fabrication process steps for gate formation.



Fig. 4 Cross sectional SEM photograph of a 0.2µm gate.

using SF₆. At this stage, the gate pattern was defined as shown in Figure 3(b). After gate region was recessed by wet etching, the gate metal (Al/Ti) was evaporated and lifted off (Figure 3(c)). By this new process, gate length was easily reduced and moreover a gate was asymmetrically formed near the source in the recess due to the overhang of upper layer photoresist. Figure 4 shows a cross sectional SEM photograph after gate metallization. A $0.2\mu m$ gate is shown in the photograph.

4. DC Performances

Table 1 shows the comparison of the DC characteristics of 0.2μ m-gate HEMTs (Wg=10 μ m) with various InGaAs thickness. As can be seen in the table, DC performances of both pseudomorphic HEMTs(InGaAs 90Å and 180Å) are excellent compared with the conventional HEMT. The maximum g_m of 490mS/mm and K-value of 664 mS/Vmm were obtained in the pseudomorphic HEMT with InGaAs thickness of 90Å. The pinchoff characteristics were also excellent, which can be seen in N_g values. This improvement may be attributed to high N_s and good carrier confinement in InGaAs well and suggests that the pseudomorphic HEMT is suitable for ultra short gate FETs.

5. Microwave Performances

S-parameter measurements were performed from 0.5 to 40GHz for the 150µm-wide devices. The short circuit current gain (h21) was extracted from the S-parameters and an f_T was determined by extrapolating h₂₁ values to unity with a slope of -6dB/octave. Figure 6 shows h21 as a function of frequency for the pseudomorphic HEMT with InGaAs thickness of 90Å. 6dB/octave gain roll-off was seen in the figure and an f_T of as high as 88.4GHz was obtained. An f_T of the device with InGaAs thickness of 180Å was a little lower (78GHz) and that of conventional HEMT (InGaAs 0Å) was about 30% lower (60GHz) than the device with InGaAs thickness of 90Å(80-88GHz). This improvement of f_T in the pseudomorphic HEMT is explained by that of DC characteristics.

	HEMTs	
with various InGaAs	thickness.	

InGaAs well width (Å)	g _{mmax} (mS/mm)	Ng*	$V_{th}(V)$
0	360	3.5	-0.41
90	490	2.3	-0.28
180	480	2.2	-0.30

* Determined from the $I_D=A \exp(qV_G/N_gkT)$ relation



Fig. 5 Frequency dependence of current gain h_{21} of 0.2µm gate pseudomorphic HEMT. InGaAs well width is 90Å.







The noise performances were measured at 12GHz for the devices with three-feeds airbridge as shown in Figure 6. Figure 7 shows a noise figure as a function of drain current. As can be seen, a noise figure of 0.49dB with an associated gain of 11.5dB is obtained at I_D=10mA in the device with InGaAs thickness of 90Å. For this device, the dependence of noise figure on drain current is considerably suppressed. This improvement can be explained by a good channel confinement and high Ns in the pseudomorphic HEMT. On the other hand, the device with InGaAs thickness of 180Å exhibits degraded noise performance. In order to explain this degradation, the dependencies of f_T and g_m on drain current were examined. Figure 8 shows f_T and g_m as a function of drain current at low drain current level. As shown in this figure, the transconductance of the device with InGaAs thickness of 180Å is lower than the device with that of 90Å especially at low drain current, and f_Ts also show the same feature. This result may be explained by gate-to-channel (2DEG) separation. The increase of N_s in pseudomorphic HEMT is almost saturated at the InGaAs thickness larger than 90Å (Figure 1), and in this region the gate-to-channel separation increase with InGaAs thickness especially at low drain current. The minimum noise figure, which is usually obtained at low drain current, is responsive to InGaAs thickness and the lowest noise figure was achieved in device with InGaAs thickness of 90Å.

6. Summary

We have demonstrated a $0.2\mu m$ gate pseudomorphic HEMT using a new gate fabrication technique. The effect of the InGaAs well width on microwave performance has been studied. Our experimental data shows the noise performance is responsive to the InGaAs thickness. The optimum InGaAs well width which minimizes noise figure is nearly 100Å and beyond this value noise performance degrades. This result was explained by the confinement of 2DEG in InGaAs well. We have achieved excellent noise performance of noise



Fig. 8 f_T and g_m as a function of drain current at low drain current level.

figure of 0.49dB with an associated gain of 11.5dB at 12GHz, and high f_{Tmax} of 88.4GHz in the device with InGaAs thickness of 90Å.

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