Extended Abstracts of the 21st Conference on Solid State Devices and Materials, Tokyo, 1989, pp. 353-356

S-A-1

Prospect of Si HBT for High Speed LSIs

Tetsushi SAKAI, Katsumi MURASE, and Shinsuke KONAKA

NTT LSI Laboratories, 3-1 Morinosato Wakamiya,
Atsugi-shi, Kanagawa 243-01, Japan

Status and future performance of Si HBTs are described. A very high-speed LSI with a basic gate delay time of less than 20ps/G will be realized using a wide bandgap emitter HBT in the near future. A narrow bandgap base HBT will be used for future Si HBT CMOS VLSIs of high performance. The Si HBT CMOS VLSIs will operate at a higher speed at low temperatures.

1. INTRODUCTION

Very high-speed LSIs are key components in information processing systems, such as main frame computers, optical transmission systems, and so on. From a practical standpoint, a silicon bipolar LSI is a very promising device because of its fast switching, high driving capability, high yield and high reliability.

The most effective way of improving bipolar transistor speed is to decrease the base width. However, thin-base transistors exhibit punchthrough phenomenon, in which the depletion layer penetrates from the collector to the emitter. This cannot be prevented by heavily doping the base without sacrificing current gain. Therefore, there is an upper limit to the base impurity concentration and a lower limit to the base width for preventing punchthrough in practical transistor operation.

An Si HBT[1] is a promising new structure that is expected to break these limits. The Si HBT is a key technology to breaking through the performance limitations of conventional bipolar transistors.

The Si HBT has two kinds of technologies, such as a wide bandgap emitter and narrow bandgap base. In this paper, the current status and future performance of Si HBTs will be described.

2. STATUS OF Si HBT RESEARCH

2-1. Wide bandgap emitter structure

An extensive research for an optimum hetero-emitter material has been made in an attempt to realize practical Si HBTs. A number of approaches have been tried over the past few years; OXygen-doped Silicon Epitaxial Films (OXSEF),[2] Semi-Insulating POlycrystalline-Silicon (SIPOS),[3] SiC,[4] a-SiC_x,[1] μc-SiC_x,[5] and μc-Si:H.[6] The properties of silicon-related hetero-emitter materials are shown in Table 1. Properties required of the hetero-emitter material include a wide band gap, a low resistivity, and a low interface state density. To introduce hetero-emitter structures into Si bipolar transistors, the necessary conditions of hetero-emitter materials were estimated for high f_T and low V_{CE} offset.

Invited by Symposium

1) A valence band discontinuity (ΔE_V) of more than 0.15 eV is determined to prevent minority carrier injection from the base to the emitter and to maintain a large f_T.
2) The heterointerface recombination, which reduces h_{FE}, scarcely influences f_T.
3) The V_{CE} offset is almost proportional to ΔE_C in low emitter concentration HBTs, indicating that emitter materials of $\Delta E_C < 0.15$ eV must be developed.

Among the several materials proposed to date, μc-Si:H and μc-SiC_x:H prepared by plasma CVD seem most promising. A current gain of 1000 is obtained with a μc-Si:H-emitter HBT(6) and a μc-SiC_x:H-emitter HBT(5).

However, the most serious problem is thermal instability in the sense that hydrogen atoms in μc-Si:H easily evolve during thermal treatment after μc-Si:H deposition. This generates an excessive base current.

Superiority of the μc-SiC_x:H-emitter HBT over the μc-Si:H-emitter HBT is the improvement in thermal stability.(5) The current gain h_{FE} versus collector current I_C characteristics of the μc-Si:H-emitter and the μc-SiC_x:H-emitter HBT's annealed at 450°C for 30 min are shown in Fig. 1. The μc-SiC_x:H-emitter HBT maintains h_{FE} well above that of the homotransistor, yielding a maximum h_{FE} of 450. The wide-gap emitter effect holds for the μc-SiC_x:H HBT even after annealing at 450°C.

2-2. Narrow bandgap base structure

The effect of reducing the bandgap in the base is to enhance the minority carrier injection into the base, resulting in an increase of h_{FE}. The bandgap graduation in a Si-Ge-base region introduces a built-in field in the base that reduces the minority carrier transit time, resulting in an increase of cut-off frequency f_T. Properties of the Si-Ge are shown in Table 1. Recently, a graded Si-Ge-base HBT(7) has been fabricated using a low temperature epitaxial silicon deposition process known as ultra-high-vacuum/chemical-vapor-deposition. The most important problem is the reduction of defect density in the Si-Ge-base region. As an example of the improved small-signal performance of Si-Ge HBT's, the record f_T for Si-based PNP's is 14 GHz.(8)

3. FUTURE PERFORMANCE OF Si HBT

3-1. Wide bandgap emitter

The common emitter cut-off frequency has been calculated using a two-dimensional device simulator.(9) The calculated results of f_T as a function of collector current density is shown in Fig. 2. f_T in homotransistors cannot exceed 50 GHz even using an optimized emitter-to-collector impurity profile, while a Si HBT is able to have a far higher f_T of 120 GHz. The speed improvements can be more easily understood if the total transit time ($\tau_{EC}=1/2\pi f_{Tmax}$) is reduced into the following five components:

$$\tau_{EC} = \tau_E + \tau_{EB} + \tau_B + \tau_{BC} + \tau_C$$

The electrical boundaries for calculating the transit time components are assumed to be the metallurgical junction boundaries in this estimation. The results for each transistor are shown in Fig. 3.

The high frequency-up procedure is mainly based on reduced base transit times, so that a technology for forming thin bases is a prerequisite for achieving high frequency Si HBT's. Utilization of a Si HBT with polysilicon self-aligned bipolar technology, with lithography of less than a halfmicron, makes it possible to achieve a basic gate delay time of less than

10ps/gate by reducing transit time τ_{EC}, including the reduction of collector-base capacitance and base resistance.

3-2. Narrow bandgap base

The cut-off frequency f_T of a Si-Ge HBT has been calculated using a one-dimensional simulator. The calculated results were 60 GHz for NPN and 31 GHz for PNP.[10] The f_T of a Si-Ge HBT is 2-3 times higher than that of homojunction transistors.

An additional advantage of HBTs is improved low temperature operation and characteristics. Si-Ge HBTs reverse the bandgap difference between base and emitter, resulting in higher current gains at liquid nitrogen (LN_2) temperature. The enhancement of minority carrier transport by a drift field is inversely proportional to kT, and thus is much larger at LN_2 than at room temperature.

BiCMOS technology can produce a VLSI that possesses the high-speed characteristics of a bipolar LSI and the low power, high packing density characteristics of a CMOS VLSI. Its power dissipation is as low as CMOS gates and the driving capability is about 5 times greater than CMOS.

The simulation results of loaded gate delay time for the combination gate circuit with advanced CMOS of L_{eff}:0.15 μm and bipolar of emitter width: 0.3 μm are shown in Fig. 4. For homojunction bipolar, if the supply voltage drops to less than 4 V, the loaded gate delay time increases exponentially. While, for Si-Ge base HBTs, if the supply voltage drops to less than 3V, the delay time increases exponentially. Superiority of the narrow bandgap base HBT over the homojunction bipolar is the improvement of operating at low supply voltage. In the case of advanced CMOSs with less than 0.5 μm rule, the supply voltage has to become lower to prevent hot electron effect. A narrow bandgap base HBT with a lower built-in voltage will be needed to fabricate future high speed and low power VLSIs with less than half submicron rule. The future performance of a Si HBT CMOS are shown in Fig. 5.

4. SUMMARY

Status and future performance of Si HBTs were described. A very high-speed LSI with a basic gate delay time of less than 20ps/G will be realized using a wide bandgap emitter HBT in the near future. The most important problem for wide bandgap emitter HBTs is improving the thermal stability of wide bandgap materials.

A narrow bandgap base HBT will be used for future Si HBT CMOS VLSIs of high performance, high speed, low power, low supply voltage and high packing density. The Si HBT CMOS VLSIs will operate at a higher speed at low temperatures.

5. REFERENCES

(1) K.Sasaki et al.; IEEE Electron Device Lett. EDL-6 (1985) 311.
(2) M.Takahashi et al.; IEEE Electron Device Lett. EDL-8 (1987) 475.
(3) T.Matsushita et al.; Jpn. J. Appl. Phys. (Suppl.) 20 (1980) 75.
(4) T. Sugii et al.; IEEE Electron Device Lett. EDL-9 (1988) 87.
(5) M.Kuwagaki et al.; Jpn. J. Appl. Phys. Lett. (1989) L754.
(6) H.Fujioka et al.; IEDM Tech. Dig. (1988) 574.
(7) B.S.Meyerson et al.; Appl. Phys. Lett. 50 (1987) 113.
(8) D.L.Harame et al.; IEDM Tech. Dig. (1988) 889.
(9) M. Ugajin et al.; Trans. IEEE Electron Device ED-6 (1989) 1102.
(10) J.M.C.Stork et al.; Symp. on VLSI Tech. (1989) 1.

Table 1. Properties of silicon-related heteromaterials

material	SiO_x		SiC_x					
	OXSEF (single)	SIPOS (uc)	SiC (single)	SiC (poly)	a-SiC_x	uc-SiC_x	uc-Si:H	$Si_{1-x}Ge_x$ (single)
ΔE_g(eV)	~0.2?	0.3-0.6	1.2	1.2	0.6-0.8	0.6-0.8?	0.5-0.8	-(0.2-0.3)
$N_d(cm^{-3})$	10^{19-20}	10^{17-18}	$2\text{-}5\times10^{18}$	10^{19}	10^{15-16}	$2\text{-}5\times10^{18}$	10^{18-20}	10^{19-20} (p-type)
ρ(Ωcm)	$10^{-(1-2)}$	10^{1-2}	$\sim10^{-2}$	$5\text{-}10\times10^{-3}$	10^{3-5}	0.1-1	0.01-1	$2\text{-}5\times10^{-3}$
deposition temp.(°C)	500-600 (MBE)	600-700 (CVD)	1000 (CVD)	800-900 (CVD)	350 (P-CVD)	400-600 (P-CVD)	350 (P-CVD)	600-800 (MBE)
transistor (h_{FE})	100(<L) 20(L)	10^3(L-M) 100(M) 10(M-H)	100(L)	diode n=1.05	300(L) 30(M)	10(L) 50(M) (PH anneal)	10^3(L) 10^2(M) 10(H)	250(L-M) 10(H)

base Gummel number (cm^{-2}): L:$\sim5\times10^{12}$, M:$\sim5\times10^{13}$, H:$\sim5\times10^{14}$

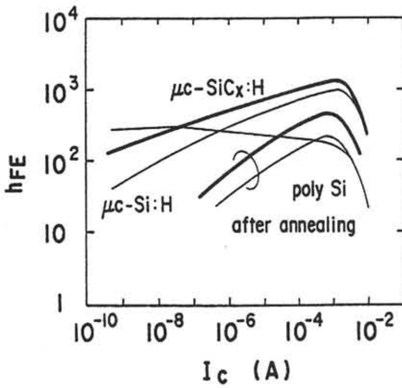

Fig.1. h_{FE} versus I_C of the uc-Si:H- and uc-SiC_x-emitter HBT's.

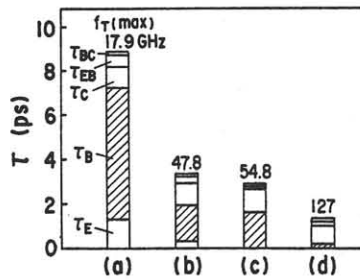

Fig.3. Transit time components.

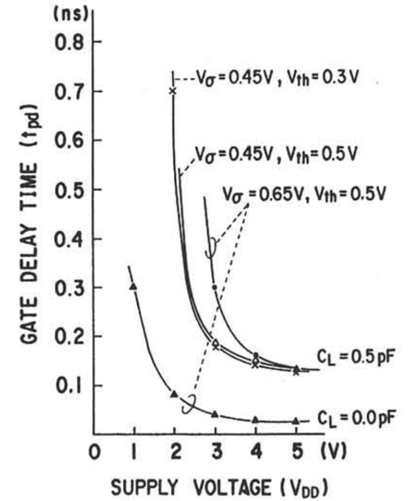

Fig.4. Loaded gate delay time for advanced CMOS and bipolar.

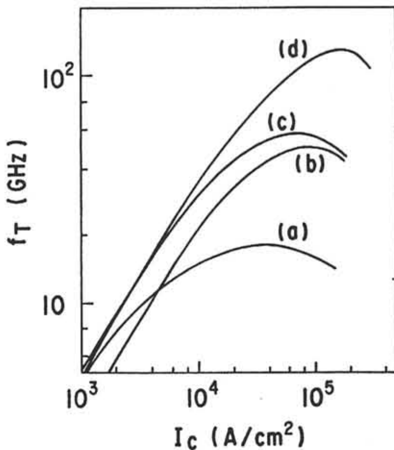

Fig.2. Calculated results of f_T as a function of I_C density.

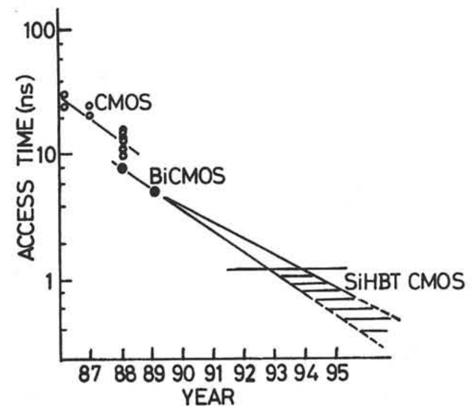

Fig.5. Future performance of Si HBT CMOS (256kbit SRAM).