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Poly-Si/GaAs Layered Structure on Si as a Wide Bandgap Emitter for Si Heterojunction Bipolar Transistor

K. Kikuta, T. Kikkawa, M. Kawanaka* and J. Sone*

NEC Corp. Microelectronics Research Laboratories
1120 Shimokuzawa, Sagamihara City, 229 Japan
*34 Miyukigaoka, Tukuba City, 305 Japan

The properties of poly-Si/GaAs layered films on Si for use in a wide bandgap emitter for Si heterojunction bipolar transistors (Si-HBTs), were studied. A smooth GaAs film surface, grown on Si, was obtained at low temperature (200°C) from the initial stage of growth. The X-Ray Diffraction (XRD) results indicated that strong GaAs orientation (111) was obtained for the poly-Si/GaAs/Si-substrate layered structure after annealing at 800°C for 20 seconds. Secondary Ion Mass Spectroscopy (SIMS) profiles indicated that impurity diffusion from GaAs layer into the p-type Si substrate was negligible at 800°C.

Introduction

Si Heterojunction Bipolar Transistors (Si-HBT) have been actively studied in recent years (1-3). The single hetero (wide bandgap emitter) Si-HBT is one of the promising candidates for high speed ULSI applications because most of its fabrication processes are compatible with those for conventional Si-bipolar LSIs.

GaAs growth on Si has been studied (4-6) but few device applications using GaAs/Si heterojunction have been reported because of the poor crystalline quality of the GaAs epitaxial films. In particular, as a result of lattice mismatch and differences in the thermal expansion coefficients between the GaAs epilayer and Si substrate, a high density of defects such as misfit, threading dislocations and stacking faults are generated at the GaAs-Si interface (7,8).

In this study, a poly-Si/GaAs/Si-substrate sandwich structure was employed to reduce the dislocation density. A very thin GaAs epitaxial layer was grown on a Si-substrate at low temperature and then an overlying Si layer was deposited on the GaAs layer by molecular beam epitaxy (MBE) without breaking the ultra-high vacuum. We fabricated the poly-Si/GaAs layered structure as a wide bandgap emitter for Si-HBT and investigated the heterojunction properties of the poly-Si/GaAs/Si-substrate.

Experiment

The poly-Si/GaAs bilayer was grown on p-type Si substrates with (111) orientation tilted 3° towards <001> direction by MBE using group IV and group III-V double chambers. Si substrates were precleaned by the RCA method ($NH_4OH:H_2O_2:H_2O=1:6:20$) and oxide sublimation was carried out at 900°C for 10 minutes in the MBE chamber. The surface after precleaning was inspected by Reflection High Energy Electron Diffraction (RHEED). The 7x7 reconstruction pattern indicating a clean Si (111) surface was observed.

GaAs films with thicknesses ranging from 10 to 600nm were grown on Si (111) substrate in the group III-V chamber in the temperature range between 200°C and 500°C and Si with a film thickness of 100nm was

successively grown on top of the GaAs films in the group IV chamber at room temperature.

The surface and film properties were investigated by Scanning Electron Microscopy (SEM), X-ray Diffraction (XRD), Secondary Ion Mass Spectroscopy (SIMS) and Transmission Electron Microscopy (TEM).

Results and Discussion

GaAs surface morphology is strongly dependent on GaAs growth temperature as shown in Fig. 1. The GaAs film thickness is about 20nm. Island growth of GaAs on the Si substrate was observed at approximately 300°C, as reported (9-11). When growth temperature was increased to 500°C, a "net"-shaped GaAs layer was grown. We found that reducing of the GaAs growth temperature down to 200°C could avoid island formation and make the GaAs surface smooth from the initial stage of growth. The crystallization of GaAs films on Si at different annealing temperatures were examined by X-ray diffraction. The diffraction intensity of GaAs (111) grown at 200°C was weaker than that of GaAs grown at higher temperatures. In order to improve the crystallinity of GaAs grown at 200°C, the poly-Si/GaAs/Si-substrate layered structure was annealed at various temperatures by rapid thermal annealing (RTA). Figure 2 shows the improvement in crystallinity after annealing at 800°C for 20 seconds. A GaAs film on Si with good surface morphology and crystallinity could be obtained by low temperature growth (200°C), followed by annealing at high temperature (800°C). Figure 3 shows a TEM cross-section of a poly-Si/GaAs/Si-substrate after annealing. The GaAs layer thickness is approximately 15nm. There are many defects in the GaAs layer. However, lattice constants of poly-Si, GaAs and Si-substrate could match

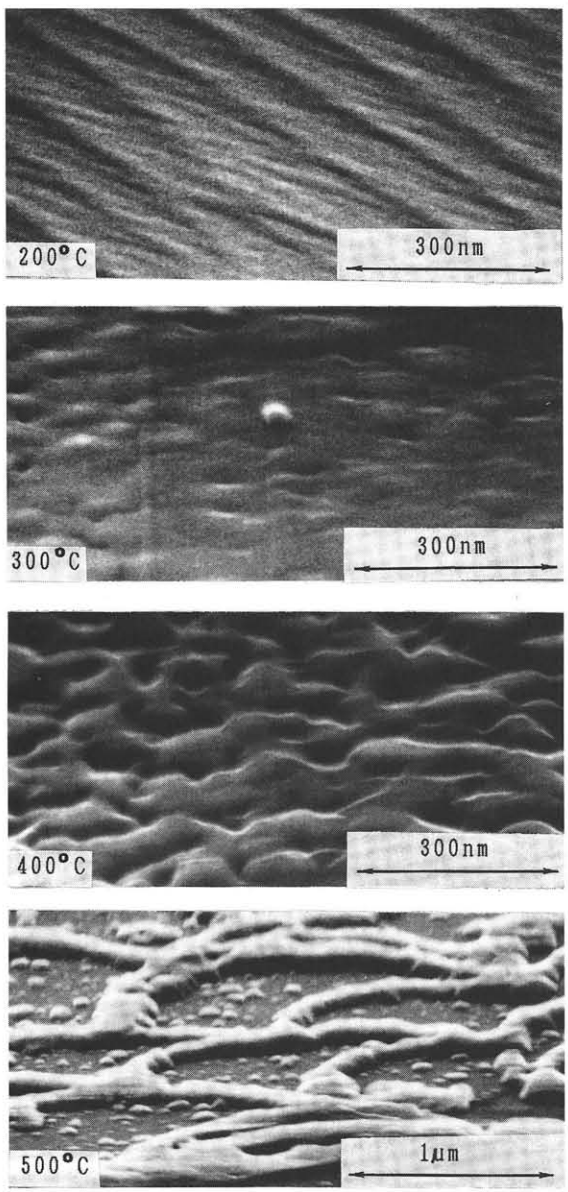

Fig. 1 The surface morphology of GaAs films on Si deposited at different growth temperatures.

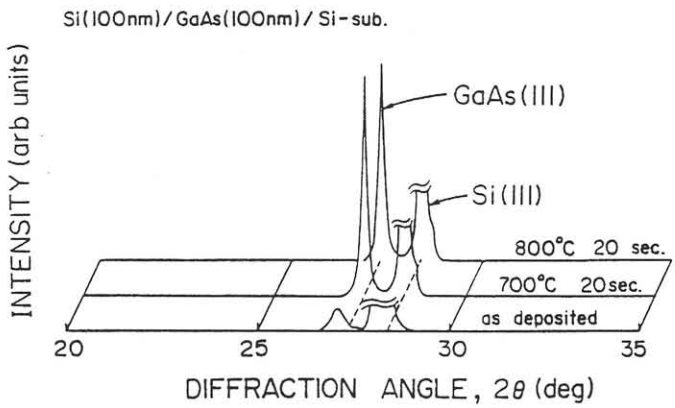

Fig. 2 The X-ray diffraction patterns for poly-Si/GaAs/Si layered films annealed at different temperatures.

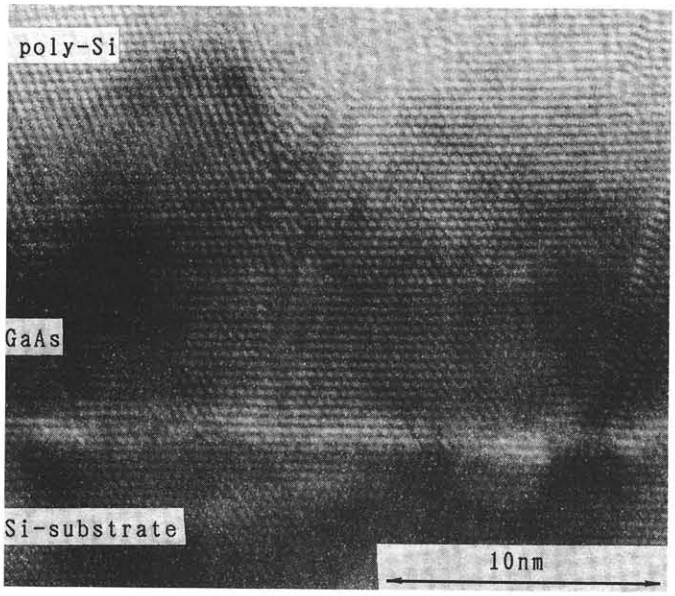

Fig. 3 The TEM cross-section of the layered structure.

locally due to distortions in the GaAs lattice matrix.

An important problem to be solved in the poly-Si/GaAs/Si-substrate structure for device applications is the interdiffusion between the Si and the GaAs layers. Arsenic is an n-type dopant for Si. If As diffuses into the p-type Si base region, a difference in position occur between the heterojunction and electrical p-n junction. This difference reduces the barrier effect of hole injection from the base into the emitter region and causes a reduction in current gain. Figure 4 shows SIMS profiles for both an as-deposited and an annealed poly-Si/GaAs/Si-substrate layered structure. These profiles indicate that neither Ga nor As diffused into the Si substrate after annealing. Therefore, the heterojunction and the electrical junction stay in the same position. Diffusion of both As and Ga from the GaAs layer into the poly-Si layer were noticeable after annealing, due to defects and grain boundaries in the poly-Si. Arsenic impurities diffuse more than Ga impurities do because As solubility in Si is greater than Ga solubility. This could make

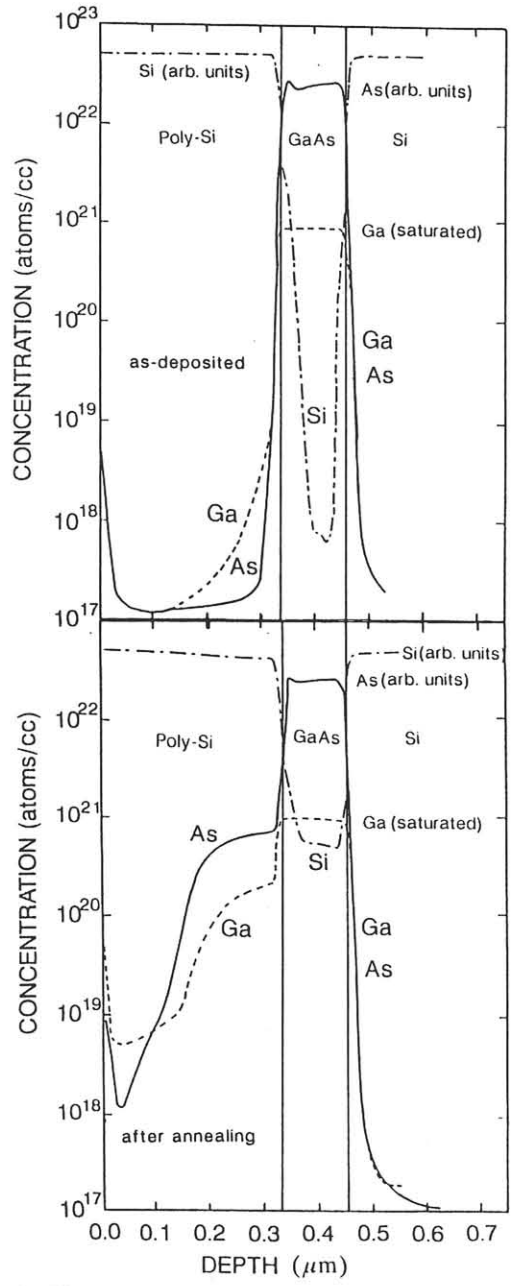

Fig. 4 The impurity profiles in the layered structure.

the poly-Si layer n-type.

Consequently, the poly-Si/GaAs layered film on Si substrate could be formed for a wide bandgap emitter of Si-HBTs.

Conclusion

We investigated the properties of a poly-Si/GaAs/Si-substrate layered structure for use in Si-HBT wide bandgap emitters. GaAs on Si with good surface morphology and crystallinity could be obtained by 200°C growth and subsequent 800°C annealing. The

interdiffusion of impurities at the GaAs/Si-substrate interface was negligible after 800°C RTA. Although there are still many defects in the GaAs layer, lattice constants of poly-Si, GaAs and Si-substrate could match locally in the sandwich structure.

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