

Reverse-Bias Current Reduction in Low-Temperature-Annealed pn Junctions Using a UHV Ion-Implanter

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The reduction in the reverse bias current in low-temperature annealed pn junctions have been studied. It was found that a transition region exists underneath the ion implantation created amorphous layer and that defects grow from this region during post-implantation anneal. Such defect growth is very much dependent upon the contamination involvement into the transition region during ion-implantation process. By performing ion implantation in ultra high vacuum environment, the leakage current level has been reduced by about one order of magnitude.

1. INTRODUCTION

Ion Implantation is a widely accepted and well established impurity doping technology in the present-day semiconductor manufacturing lines. However, when it is aimed to form shallow junctions by reducing the annealing temperature, a large increase in the reverse-bias current has been observed. The reverse-bias current level obtained by 600°C annealing, for instance, is $\sim 10^{-5}$ A/cm², which is more than four orders of magnitude larger than that obtained at temperatures above 900°C^(1,2).

The purpose of this paper is to clarify the mechanism of the reverse current increase in low temperature-annealed pn junctions through a series of cross sectional transmission microscope (XTEM) studies. It will be shown that the contamination involvement during the ion implantation process has a critical effect on the defect formation at a pn junction interface. The reduction in reverse-bias current for low-temperature-annealed pn junctions by using ultra high vacuum⁽³⁾ (UHV) ion implanter will be demonstrated.

2. EXPERIMENTAL

The UHV ion implanter utilized in this experiment has a back-ground pressure of 10^{-10} Torr, and employs ultra clean gas delivery system for the ion source⁽³⁾.

p-type(100) silicon substrates having resistivity of 0.4~0.6 Ω cm or 3~8 Ω cm were used for pn junction formation or for carrier concentration measurement and TEM studies, respectively. Arsenic ions were implanted typically at 105 keV with a dose of 6×10^{15} /cm² either into bare silicon surfaces or through a 100 Å thick thermal oxide. Post implantation anneal was performed in nitrogen ambient at temperatures of 550°C~1000°C, for 30~75 min. In order to visualize the ion-implanted regions before and after the anneal, cross-sectional transmission microscope (XTEM) studies were carried out. The carrier concentration profiles were obtained by repeating the anodic oxidation and the four point probe measurement.

3. RESULTS AND DISCUSSION

Figure 1 shows the carrier concentration profile in arsenic-implanted silicon as a

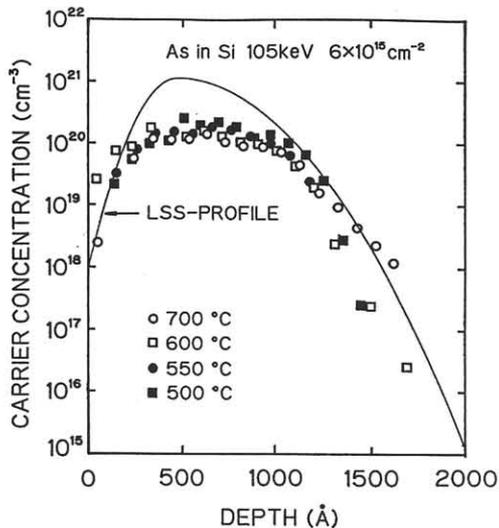


Fig.1 Carrier concentration profiles in As-implanted silicon after annealed in N_2 for 75min. The solid line represents the calculated LSS impurity profile.

function of annealing temperature. Although no appreciable impurity diffusion occurs below 600 °C, a small amount of diffusion is evidently observed in the sample annealed at 700 °C. In the sample annealed at 1000 °C, a large impurity diffusion was observed and the junction depth was approximately 0.3 μm .

Figure 2 demonstrates the XTEM micrographs of arsenic implanted silicon before ((a),(b)) and after ((c),(d)) the thermal anneal. The top pictures show the samples implanted through 100 Å thermal oxide while pictures at the bottom represent bare silicon implanted samples. In as implanted samples, it is observed that a transition region exists between the ion implantation-generated amorphous layer and the substrate. The width of the transition region is about 300 Å or 500 Å for thru-oxide implanted or bare-surface implanted samples, respectively. The existence of such a transition region indicates the interface between the ion implanted layer and the substrate is not an abrupt transition from amorphous to single crystal. The transition region would be a highly defective region of silicon.

On the other hand, for samples after

thermal annealing, it is seen that a large amount of defects extend from the transition region not only into the regrown layer but also into the substrate. Furthermore, it is very important to note that much higher density defects are existing in the thru-oxide implanted sample. From these pictures, it is known that defects in the transition region grow to secondary defects such as dislocation loops during post implantation anneal and contribute to the increase in the reverse-bias current. In spite of such high density defect generation, the reverse-bias current level of 1000 °C annealed n^+p junctions is very small. This is because these defects are included within the n^+ layer which expanded by the thermal diffusion of implanted arsenic. The problem of such defect generation is much more significant for low-temperature annealed n^+p junctions, since the impurity diffusion at low temperature is negligibly small as shown in Fig.1. The grown defects are included in the depletion region of a reverse-biased n^+p junctions, increasing the reverse-bias current.

Higher defect density found in the thru-oxide implanted sample indicates that knock-on implanted oxygen atoms could enhance such defect generation. This means that the defect generation would be a combined effect of a highly defective transition region and the contamination species incorporated into the transition region. Therefore, the elimination of any kind of contamination involvement into the ion implanted region is of paramount importance to suppress the defect generation and to realize low-reverse-current n^+p junctions.

Figure 3 shows the dependence of reverse-bias current on annealing temperature. Arsenic implantation was performed into bare silicon surfaces under

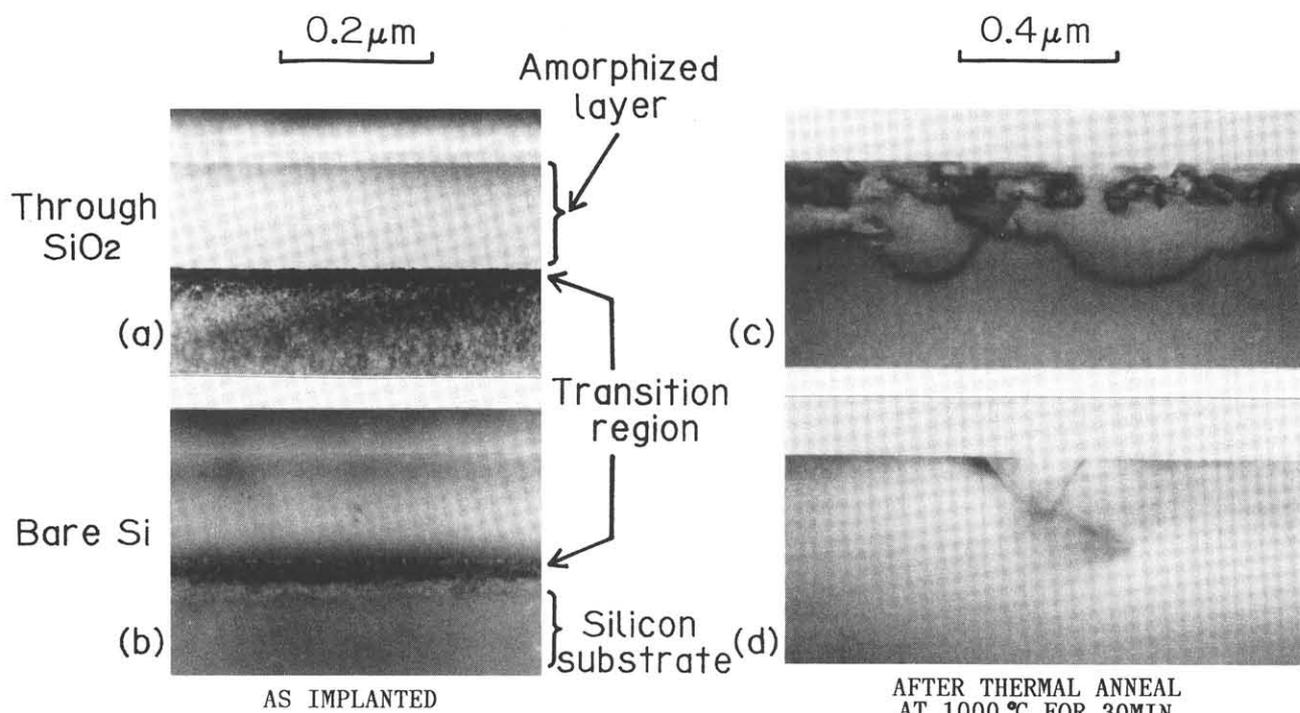


Fig2. Cross sectional TEM micrographs of arsenic implanted silicon before ((a),(b)) and after ((c),(d)) the thermal anneal. The top pictures show the samples implanted through 100Å thermal oxide while pictures at the bottom represent bare silicon implanted samples. Here, the acceleration energy and the dose for As implantation was 120KeV and $1 \times 10^{16} \text{cm}^{-2}$, respectively.

two different base pressures, viz., 5×10^{-10} Torr and 1×10^{-7} Torr. Definite difference in the reverse bias current was observed in n^+p junctions formed under different vacuum conditions. Especially at the temperature range of 800 to 900 °C, the reverse-bias current was reduced by about one order of magnitude under the high vacuum condition. However, apparent difference was not observed for samples annealed below 700 °C.

The reverse-bias current data shown in Fig.3 were separated into two components, i.e., the peripheral current density component and the areal current density component. The temperature dependence of the areal current density component is shown in Fig.4, where the data for n^+p junctions formed at 25 keV under ultra high vacuum is also presented. More than one order of magnitude improvement in the reverse bias current level is seen for samples annealed at 800 °C and 900 °C by UHV

implantation. Further reduction in the reverse current is obtained for samples implanted at 25 keV. The reduction in the reverse current observed in samples implanted under UHV conditions is interpreted as that the contamination involvement due to the residual gas adsorption onto the silicon surface and their recoil implantation into the transition layer have been decreased.

We have found that many kinds of contamination are generated by high energy ion beam sputtering occurring in the ion-implantation system through the SIMS and XPS analysis. Such contaminant species when incorporated into the transition region also contribute to the generation of defects. In order to eliminate such sputtering contamination to wafers, we installed sputtering protection apparatus in the ion implanter. As a result, further reduction in reverse bias current was achieved. Approximately one order of magnitude

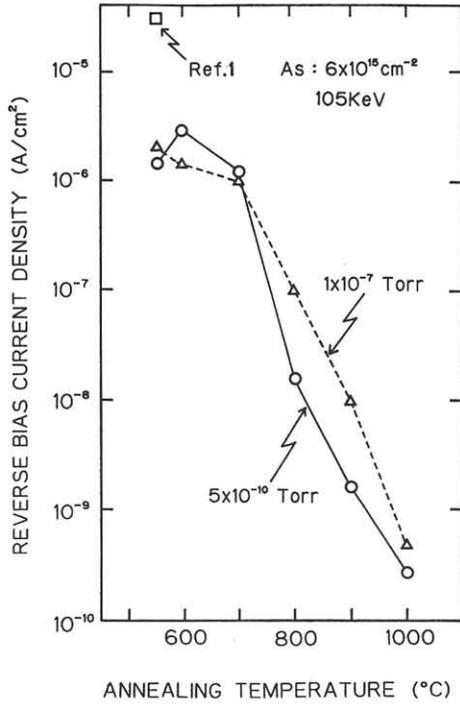


Fig.3 The reverse-bias current at a reverse bias voltage of 5V as a function of annealing temperature. Arsenic implantation was performed into bare silicon surfaces under two different base pressures, viz., 5×10^{-10} Torr and 1×10^{-7} Torr.

reduction in reverse bias current as compared to the UHV data shown in Fig.3 has been obtained not only for samples annealed at 800°C, but also for samples annealed below 700°C. The total reverse currents including the peripheral component (at a reverse bias voltage of 5V) for 600°C and 700°C annealed junctions were 3.1×10^{-7} and 1.7×10^{-7} A/cm², respectively.

4. CONCLUSIONS

The reduction in the reverse bias current in low temperature annealed pn junctions have been studied. It was found that a transition region exists underneath the ion implantation created amorphous layer and that defects grow from this region during post-implantation anneal. Such defect growth is very much dependent upon the contamination involvement into the transition region during ion-implantation process. By performing ion

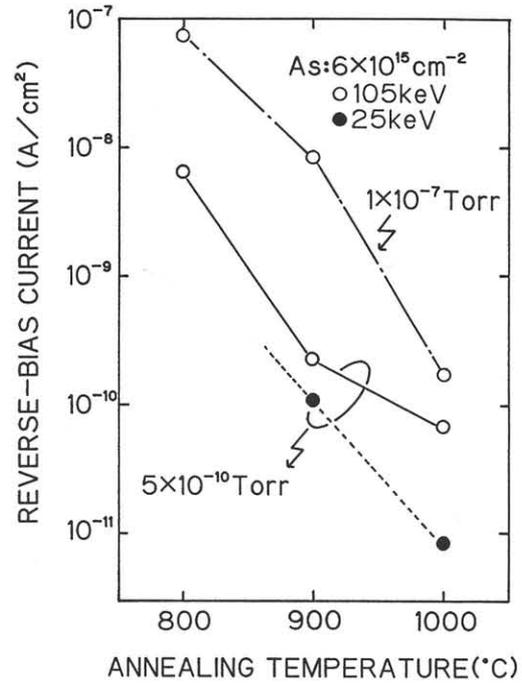


Fig.4 The areal leakage current component extracted from the data shown in Fig.3 as a function of annealing temperature. The data for n⁺p junctions formed at 25KeV under high ultra high vacuum is also included.

implantation in ultra high vacuum environment, the leakage current level has been reduced by about one order of magnitude. Further reduction in the reverse bias current has been achieved by introducing sputtering protection apparatus that eliminates wafer contamination due to the high energy sputtering of components in the ion implantation system.

5. ACKNOWLEDGMENT

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6. REFERENCES

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