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GaAs/AlGaAs Optical Interconnection Chip for Neural Network

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An optical synaptic interconnection device has been fabricated using GaAs/AlGaAs technology. It consists of a light-emitting-diode array, an interconnection matrix and a photodiode array, which are integrated in a hybrid-layered structure on a GaAs substrate. The LED array and PD array with good uniformity have been fabricated with molecular beam epitaxy (MBE). Mulitiple quantum well (MQW) active layer and Bragg reflector were employed to obtain high efficiency of the LED. The device structure and characteristics are reported in detail. The fabricated device was used to simulate neural network system with 32 neurons. The associative memory was successfully implemented.

1. INTRODUCTION

The area of neural networks has a good chance of realization for pattern recognition, associative memory and error correction.[1] While computer simulation studies have been advanced, actual implementation using electronics[2),3)] and optics[4),5)] has been developed slowly. Though electronics implementation seems rather realistic at present stage, optics should be superior due to the inherent parallelism of optics.[6)]

In this paper, we describe an optical chip[7)] for the synaptic interconnections. It has remarkable features that are good mechanical stability, compactness in size, and compatibility to electric circuits, compared to the reported system composed of discrete devices. It consists of three stacked layers, which are a light-emitting-diode (LED) array, an interconnection matrix and a photodiode (PD) array. The fundamental function of this chip is to perform a multiplication of a vector with 32 elements and a matrix with 32x32 elements in parallel. By combining this chip with external electrical nonlinear thresholding devices and feedback circuits, we have demonstrated an associative memory based on Hopfield neural network model.[8)] Furthermore, we describe the fabrication and performance of the LED array and PD array. The LED array fabricated by MBE consists of GaAs/AlGaAs MQW active layer and AlAs/GaAs Bragg reflector and the PD array consists of MQW absorption layer.

2. STRUCTURES and FABRICATION

The schematic drawing of the chip is shown in Fig. 1. This chip consists of three

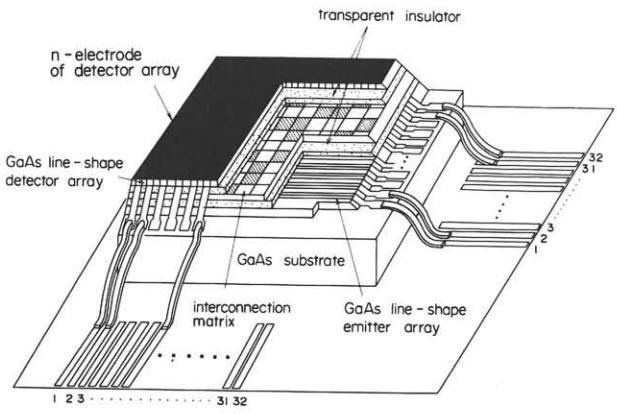

Fig. 1 Schematic diagram of GaAs/AlGaAs optical synaptic chip.

stacked layers. The line-shaped LEDs and PDs are placed in a cross-bar structure with the interconnection matrix elements sandwiched between them. As the result, vector-matrix multiplication,

$$u_i = \sum_{j=1}^{N} T_{ij} v_j \qquad (1)$$

is accomplished in parallel. Here, the vector v_j, T_{ij} and u_i represent the state of j-th LED, the optical transmittance of (i,j)-th interconnection matrix element and the photocurrent of i-th PD, respectively.

MBE was used to grow the following epitaxial layers on n-GaAs substrate so that uniform characteristics were obtained over large areas of the LED and PD arrays. The LED consists of six layers which is shown in Fig. 2; a 0.1μm n-GaAs buffer layer, Bragg reflector consisting of 10 pairs of AlAs/GaAs quater-wavelength stack, a 1μm n-$Al_{0.3}Ga_{0.7}As$ confinement layer, an undoped active layer consisting of 5 pairs of 10nm quantum wells with 10nm $Al_{0.3}Ga_{0.7}As$ barrier layers, a 0.5μm p-$Al_{0.3}Ga_{0.7}As$ confinement layer, and a 50nm p^+-GaAs contact layer. Bragg reflector which has a reflectivity of 90% at the center wavelength (λ=880nm) was used to take out LED output power efficiently. The PD consists of four layers; a 0.1μm n-GaAs buffer layer, a 0.5μm n-$Al_{0.3}Ga_{0.7}As$ confinement layer, an undoped absorption layer of 33 pairs of 15nm GaAs quantum wells with 15nm $Al_{0.3}Ga_{0.7}As$ barrier layers, a 0.1μm p-$Al_{0.3}Ga_{0.7}As$ confinement layer, and a 50nm p^+-GaAs contact layer. To fabricate the LED and PD arrays, both wafers were mesa-etched using chemical etching after the growth. A 0.1μm SiO_2 film was oposited on the entire wafer by plasma enhanced chemical vapor deposition to isolate electrically each LED and PD mesas of the array. Next, the SiO_2 films were etched to form stripe windows for the LEDs and PDs, respectively. The Cr/Au Ohmic contacts were formed on the top of the mesas leaving an optical access window in the middle of the mesas. Then the binary interconnection matrix was patterned on both the LED and the PD using a standard lift-off process on the surface of each mesa. The size of the each pixel was 100μmx10μm and 100μmx100μm, respectively. The arrays of the LEDs and PDs cleaved from the wafers were flip-chip bonded. The additional electrical isolation between two chips was provided by quater-wavelength SiO_2 layers which served as anti-reflection coating. The integrated chip with a size of 8mmx8mm was mounted on the flat package with 128-pins.

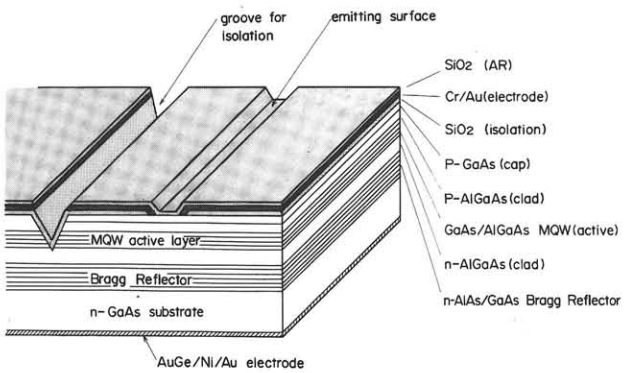

Fig. 2 Schematic diagram of the surface emitting MQW LED array.

3. DEVICE CHARACTERISTICS

Figure 3 shows the whole emission pattern of the LED array through the interconnection matrix consisting of 32x32 elements. Each of the 32 rows in the array was wire-bonded on each side of the LED electrode. The line scan picture below the micrograph demonstrates power output uniformity of the LED array along the mesa. The power distribution along one row of the array was about 5% which is attributed to uniformity of the crystal growth and the optimum design of the LED.

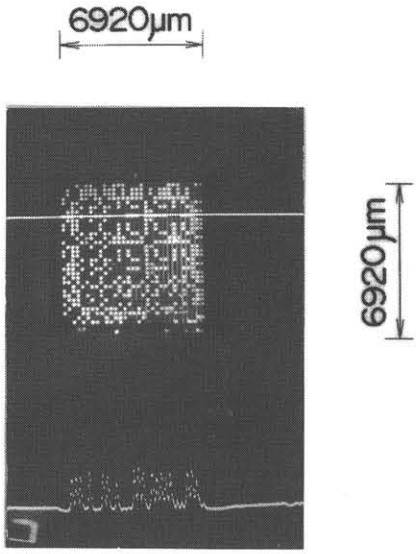

Fig. 3 Emission pattern of the LED array through the interconnection matrix T_{ij}(-).

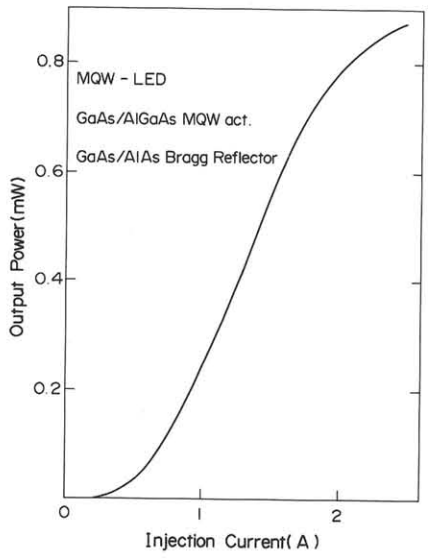

Fig. 4 Power output versus current for the LED array whose near-field pattern is shown in Fig. 3.

Figure 4 is a plot of the power output versus current for the array whose near-field pattern is shown in Fig. 3. The light output was sublinear with the injection current. As the array was not temperature controlled, the power output showed the saturation due to temperature rise.

As the LEDs and PDs are placed in a cross-bar structure, vector-matrix product can be detected as the photocurrent of each row of the PD array. The total input optical power per one row of the PDs was about 15μW, and the corresponding total photocurrent was about 1.6μA resulting in the sensitivity of about 0.1A/W.

4. OPTICAL SYNAPTIC DEVICE CHARACTERISTICS

In this section, we describe the characteristics of the chip as a vector-matrix multiplier and its application to the associative memory using the chips as the synaptic interconnection in the neural network. The precision of the vector-matrix multiplication is determined by the optical crosstalk which in turn degrades the system performance in some networks. The optical crosstalk is defined as the ratio of the stray light which leaks out from neighboring LED elements to the light which enters directly in front of the LED element. The optical crosstalk was measured as the photocurrent of one row of the PD array to be about -13dB, whereas the numerical calculation showed smaller values for the ideal device configuration. The optimum design of the apertures of the LED and PD, and T_{ij} pattern will lead to the reduction of the optical crosstalk. The computer simulation also showed that the optical crosstalk would not influence the performance of the associative memory when it is below -10dB.

The response speed of the optical synaptic interconnection chip was measured by monitoring the temporal variation of the PD current in response to the input driving

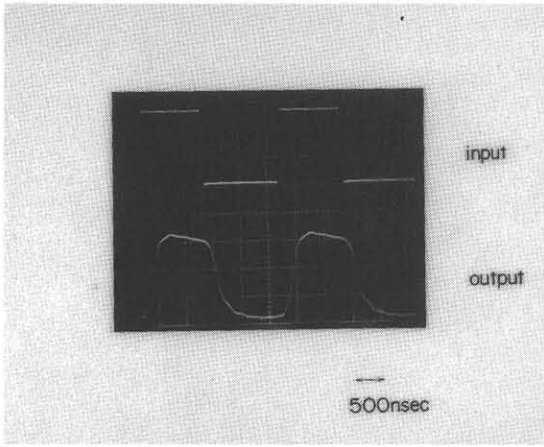

Fig. 5 The measured response characteristics of the optical chip. Top trace is input pulse and bottom trace is photocurrent of the PD. Horizontal scale is 500ns/div.

current pulse of 30mA into the one LED. Figure 5 shows the input pulse and the measured photocurrent. The observed rise time was 0.2μs with 0.4μs fall time. By reducing the size of the PD element, higher speed response could be easily obtained.

The Hopfield associative memory with 32 neurons was constructed by combining the chip with the external electronic circuits. Three complete vectors $v_i^{(m)}(m=1,2,3;\ i=1,2,..,32)$ were stored in the optical interconnection matrix. Two optical synaptic chips corresponding to the positive ($T_{ij}^{(+)}$) and the negative ($T_{ij}^{(-)}$) elements of the bipolar T_{ij} matrix were required to implement the matrix-vector multiplication. After the corresponding outputs from the two synaptic chips were processed by the differential amplifiers, they were compared with the externally applied threshold values by comparators. The outputs were fedback in parallel to the inputs of two synaptic chips.

The recognition rate was averaged over randomly selected 100 input patterns for each Hamming distance 'd'. In response to all the partial inputs with d=1, the correct vectors were retrived. However, in the case of d=4, the recognition rate was degraded down to about 70%, whereas the computer simulation shows no degradation for this Hamming distance. This result is presumably attributed to the accumulated influence of the optical crosstalk, the non-uniformity in the power distribution of the LEDs and the non-uniformity in the responsivity of the PDs.

5. SUMMARY

We describe the fabrication and performance of the optical synaptic interconnection chip consisting of 32-LED array and 32-PD array. This is the first demonstration of optical neurochip. Very uniform light output for the LEDs has been obtained. Furthermore, we have demonstrated the associative memory based on the neural network model by using this chip which has 32 neurons. The extension of this approach will allow us to implement very large neural network.

6. REFERENCE

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