

Vertical to Surface Transmission Electro-Photonic Device for the Application of Optical Interconnection and Processing

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Electro-photonic incorporation in the VSTEP permits a dynamic reconfiguration of optical interconnections, which is a significant function in optical switching and computing systems. It is because non-linear characteristics are electrically controllable in the VSTEP. Variable optical interconnection, one example of the dynamic reconfiguration, has been successfully achieved in a pnpn-VSTEP array through a matrix operation. High-speed electric addressing of 1ns per one element has been confirmed.

1. Introduction

The optical beam propagation properties of mutually noninteracting photons are expected to offer massively parallel interconnection and information processing capabilities desired for optical switching and computing systems. Vertical to Surface Transmission Electro-Photonic device (VSTEP), based on the concept of the electro-photonic incorporation, has yielded drastic improvement in power consumption and characteristics uniformity. Their successful monolithic integration in a 1K-bit level with such functions as memory, thresholding, and logic operations has been reported¹.

Another functions such as variable optical interconnection, or variable spatial light modulation (SLM), over a two-dimensional array, however, are also important. The electro-photonic configuration in the VSTEP is expected to realize these dynamic reconfiguration functions easily, because non-linear characteristics are electrically controllable. A VSTEP with an electronically selective multiple output port, which has a laser cavity structure, has been reported².

One dimensional VSTEP arrays in combination with a fixed photo-mask has been applied in an optical crossbar interconnection experiment³. This paper reports the two-dimensional pnpn-VSTEP array with a variable optical interconnection function, which was permitted through a matrix operation.

2. Device Structure

Figure 1 shows one element structure⁴⁻⁸ in two-dimensionally integrated NxN pnpn-VSTEP array. The epitaxial layers were grown on a semi-insulating GaAs substrate by molecular beam epitaxy in the following order: an n-GaAs buffer layer (0.5 μ m, $2 \times 10^{18} \text{cm}^{-3}$), an n-Al_{0.4}Ga_{0.6}As (1 μ m, $5 \times 10^{17} \text{cm}^{-3}$), a p-GaAs (50 \AA , $1 \times 10^{19} \text{cm}^{-3}$), an n-GaAs switching layer ($1 \times 10^{17} \text{cm}^{-3}$, 0.3 μ m), an n-GaAs active layer ($4 \times 10^{18} \text{cm}^{-3}$, 0.7 μ m), a p-Al_{0.4}Ga_{0.6}As (0.5 μ m, $5 \times 10^{18} \text{cm}^{-3}$) and a p-GaAs contact layer (0.15 μ m, $1 \times 10^{19} \text{cm}^{-3}$). A pnpn-VSTEP exhibits thyristor-like electronic nonlinearity. The switching layer has been added to allow independent optimization of switching voltage and optical response in the light emitting diode mode emission. As a result the optical rise time of 6ns was

obtained without changing the switching voltage V_s of $2.4V^1$. The holding voltage V_H was around $1.6V$. The cell size was $30\mu m \times 30\mu m$. Independent electrodes were formed both for anode lines and cathode lines, so that an individual VSTEP element might be driven independently by selecting anode and cathode lines going to the corresponding element.

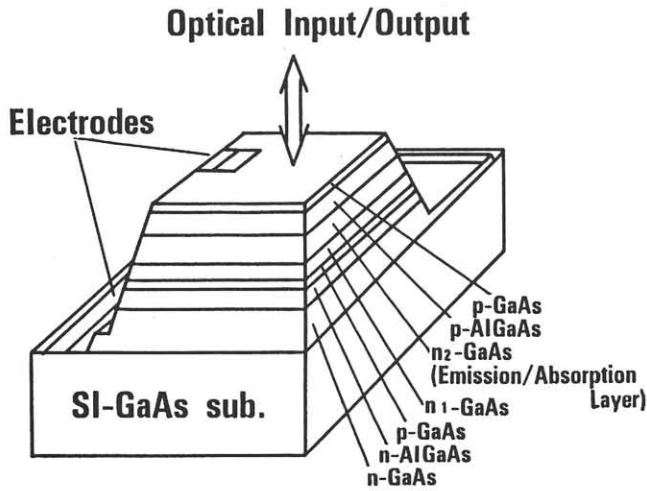


Fig. 1 Structure of a pnpn-VSTEP

3. Variable optical interconnection through a Matrix Operation

The operation scheme for variable interconnection in two-dimensional pnpn-VSTEP array is shown in Fig. 2. Electronic addressing signals ($V_1: 0 < V_1 < V_A$) are applied in turn parallel to anode lines biased greater than the holding voltage V_H , synchronized with electronic control signals ($V_2: -V_B < V_2 < 0$) applied to cathode lines. V_A is the maximum value applied to an anode line, and $-V_B$ is a minimum value applied to a cathode line. One pnpn-VSTEP, where both an addressing signal and a control signal are applied simultaneously, switches on. Input electric data are, then, sent to anode lines. Modulated light emission takes place vertical to surfaces in accordance with the addressing. The addressing can be erased by an application of negative reset pulses to all anode lines.

Using the matrix operation, N^2 optical

interconnections (in this case 0 or 1) can be reconfigured and programmed through $2N$ electric control lines. This alleviates the dynamic reconfiguration procedure greatly, in particular, when N increases. While electronic interconnections are often subject to planar geometrical constraints, optical interconnections suffer no such limitations. Multiple interconnections with high density of N^2 may become possible through vertical to surface optical interconnections with no physical contact.

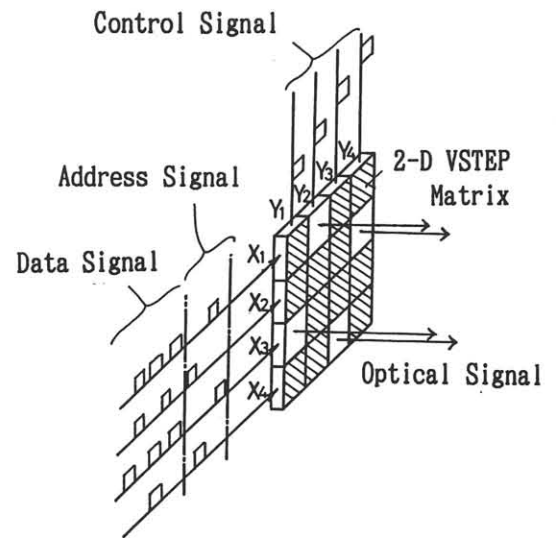
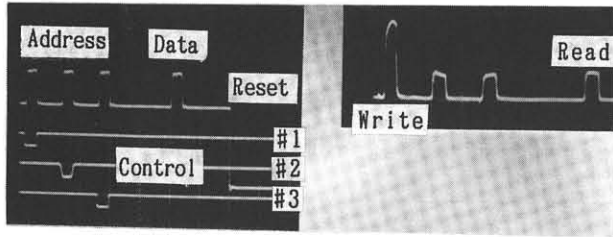


Fig. 2 Variable interconnection using 2-D VSTEP

4. Experimental Results and Discussion

Using VSTEP elements in one anode line of a 8×8 matrix, above mentioned matrix operation was carried out. In an addressing period, three sequential pulses, synchronized with control pulses applied to cathode lines, were sent to the anode line in order to switch on three elements. A signal pulse and a negative reset pulse were added behind the addressing period (Fig. 3(a)). Figure 3(b) shows a current response of the first element, which shows an expected normal response. Similar normal response was also confirmed for other elements. The time, which is required to electronically switch on one VSTEP, is dependent on a delay time in the switch-on. This delay time is shortened with

the increase in the voltage applied between an anode and a cathode. Although the maximum voltage may be considered to be $V_A + V_B = 2(V_S - V_H)$ statically, larger voltage was found to be necessary due to the delay time in the switch-on (Fig. 4).



(a) Driving pulses (b) Current response of the first element (Vert. 2mA, Horiz. 100ns/div)

Fig. 3 Write, Read, Reset Operation

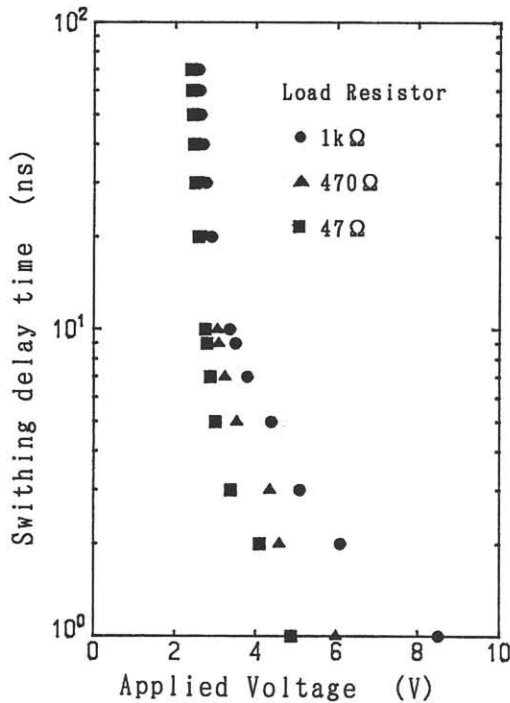


Fig. 4 Voltage dependence of switching delay time

A load resistor acts as a current limiter. Increase in a load resistor causes a voltage drop there. A resultant longer delay time could be shortened by an application of higher voltage. In the case of

1kΩ load resistor switch-on time of 1ns was realized by an application of a voltage almost three and a half times larger than V_s . Voltage drop due to an internal line also influences the delay time, which should be taken into account. Assuming the addressing of 32x32 (=1,024) matrix with 1kΩ load resistor, internal line resistance between adjacent elements must be lowered to 0.1Ω, where the delay time of 1ns can be expected with a bias voltage of 3.7Vs (Fig. 5).

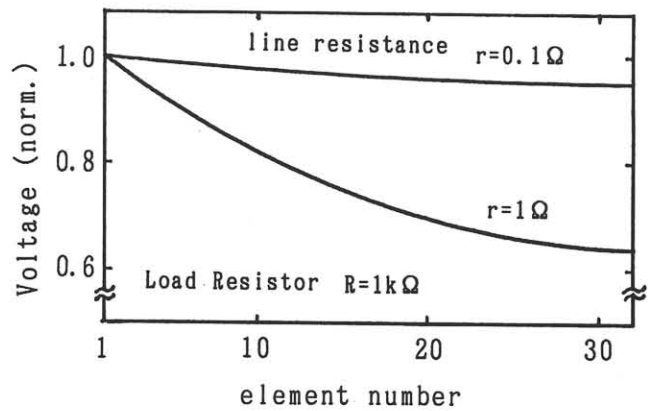


Fig. 5 Result of Simulation

Figure 6 shows a result of the reconfiguration of a part of optical interconnections, which was done sequentially.

Extended version of variable optical interconnections enables simultaneous multiplexing with the weighting and their summation, changing the values of weighting. This kind of interconnection with addressing function may be expected to be important to the application of two dimensional optical switching or optical neural computing.

5. Conclusions

Non-linear characteristics of a VSTEP are electrically controllable. A dynamic reconfiguration of optical beams, which is one of the important functions in optical

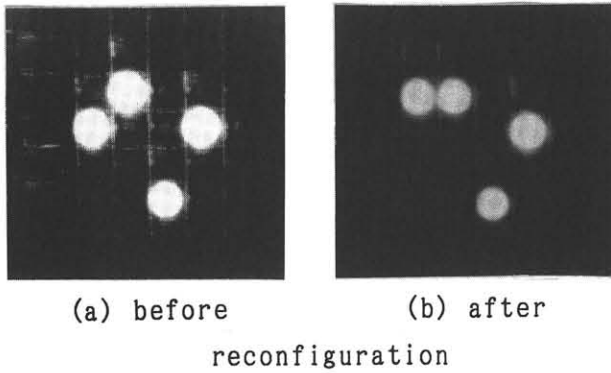


Fig.6 Reconfiguration of optical interconnection

switching and computing systems, thus, has been easily realized. Variable optical interconnection, one example of the dynamic reconfiguration, has been successfully achieved in a pnpn-VSTEP array through a matrix operation.

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